Development of low power front-end electronics for monolithic Active Pixel Sensors

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Development of low power front-end electronics for monolithic Active Pixel Sensors

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Dedicated to my loving grandmother
who inspired me to reach my personal goals
and to my amazing family
for their important support during all these years

Abstract

The next generation High Energy Physics experiments require the development of novel radiation sensor technologies adequate to cover very large areas and suitable for extreme radiation conditions. In this field, thanks to its incomparable properties, silicon is still nowadays the dominant semiconductor used to build tracking detectors for ionizing particles. In several experiments all around the world, it is used to cover very large areas with the intent of tracking and identifying the crossing particles generated during the experiments. Different topologies of silicon sensors can be used for these applications but those commonly used for high rate environments are pixel sensors. This research activity focuses mainly on two particular types of these sensors: hybrid pixel sensors and monolithic active pixel sensors (MAPS). Modern detectors use intensively hybrid sensors due to their excellent properties. This technology indeed allows to develop sensor and electronics separately allowing a very effective optimization of each part of the device increasing in this way its versatility and allowing to meet most of the requirements of the new experiments. The hybrid technology is fast and also suitable for working in high radiation environments thanks to the use of high electrical fields for the charge collection. However, the production cost of those devices is much higher than other sensors because two different devices are required and also due to the additional cost for the bump bonding used to interconnect sensor and readout ASIC. On the other hand, monolithic sensors are based on the implementation of sensor and readout electronics in the same silicon wafer. Therefore this technology is much cheaper than the hybrid solution and allows to reduce significantly contribution of the detector to the material budget. However, traditional MAPS have some limitations in terms of speed, extension of the depletion volume, signal to noise ratio and radiation tolerance which make those devices unsuitable for the extreme environment of the new experiments.

In this context, this work presents the development of a full depleted monolithic pixel sensor with a thickness of 300 μm which aims to overcome the main limitations

of the conventional monolithics. The proposed device has properties similar to the hybrid solution but benefits of the low production cost typical of monolithics. The development of the device has been carried out by the collaboration between the University of Trento, INFN of Padova and INFN of Torino. In addition, thanks to the close collaboration with the experts of a silicon foundry, it was possible a tailored fabrication of the devices. Two ASICs of 2 mm $\times$ 2 mm have been developed in a customized *double-sided* CMOS technology with transistors of 1.2 V and 6 metal layers. The devices have been submitted to the foundry for fabrication on April 2016 and have been delivered for the testing phase on May 2017. A patent for the device has been granted in 2017. In the first part of this work, the state of the art of monolithics is given where hybrid and monolithics are compared. Then, the novel sensor is described in detail with the support of simulations to motivate important solutions adopted to reach the full depletion and to implement PMOS transistors avoiding the competitive charge collection. Some studies to highlight the huge limitations on design MAPS without access to the process data are presented to introduce the custom process used for the development of the device. The first ASIC is a test chip designed to contain test devices used to study important properties of the sensor like depletion and punch-through voltage. All the devices implemented in this ASIC are described in detail motivating the design solutions adopted. The second ASIC is the complete monolithic sensor called MATISSE (Monolithic AcTIve pixel SenSor Electronics) made by a matrix array of 24 $\times$ 24 pixels readout with the snapshot shutter technique. Each pixel is 50 μm$\times$50 μm and is based on the same novel sensor. The chip is described in detail with the support of simulation results to motivate some strategies adopted during the design. Special emphasis is placed on the strategy used to design the readout chain with a wide output swing, low noise and excellent linearity with the use of high threshold transistors. Last but not least, in the last chapter the results collected during the characterization of the two prototypes for different wafers are presented. The data acquisition system developed is described and the electrical tests and measurements with active sources and lasers are reported. The measurements performed on the test structures show unwanted trapped charge in the backside oxide. The phenomenon is described putting special attention on an irradiation campaign performed in the test diodes to confirm and quantify this effect. All the results presented in this work aim to prove the device full depletion and the excellent properties of the embedded electronics implemented in these first prototypes.

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Chapter 1

Monolithic active pixels sensors

Silicon has been used intensively since 1970s as the main material to built vertex and tracking detectors for High Energy Physics (HEP) experiments. Among semiconductors, this element is abundant in the Earth crust and for this reason it is very cheap. The low cost together with the well known technology used for the extraction, the purification and to process the raw material, made the silicon technology the predominant solution to built detectors for particle physics.

Silicon pixel sensors are one example of silicon detectors used in this field. Thanks to their small size and to the growing progress of electronics, those devices are suitable especially to build the innermost layers of silicon trackers where the radiation level can be up to a Grad and the expected particle rate can reach values of 1 GHz/cm^2 as it will be in the case of the High Luminosity Large Hadron Collider (HL-LHC). Two different technologies can be used to built these devices. The first technology is the hybrid one which is based on a device made of two independent layers. The first layer is the sensitive volume and is typically a silicon sensor. The second layer is the readout ASIC (Application Specific Integrated Circuit) which is developed in a standard CMOS (Complementary Metal Oxide Semiconductor) process technology. Since the layers are produced separately, they can be built by using different materials and technologies allowing to get a very effective device optimization. The second technology is called monolithic because the device is made as single block. Pixel sensors with an active electronics on board realized with this technology are called Monolithic Active Pixel Sensors (MAPS) and are based on one single layer where both, the sensitive volume and the CMOS readout

electronics, are built. Since only one production step is needed for the device fabrication, this technology is generally much cheaper than the hybrid one. So far the hybrid technology has been the mainstream in HEP in spite of its cost, because its better performances. However, the next generation of experiments requires the development of new radiation silicon sensor technologies to cover very large areas and the cost is becoming an important factor to take carefully into account. For this reason, several R&D activities started around the world to improve the performance of conventional monolithic sensors to make them suitable for the new generation of experiments.

In this chapter the properties of the conventional monolithic sensor are described. Before this description, the first section of this chapter is dedicated to give the basic concepts of silicon sensors needed for the description of these devices. Here, the concepts of sensor depletion and signal generation are discussed. After this introduction, the monolithic technology is described and some examples of existing monolithics will be given. In this description a comparison between the monolithic and the hybrid technology is also proposed to highlight the main differences between these sensors.

1.1 Basic concepts of silicon pixel sensors

The theory of semiconductors is the key to understand the behaviour of silicon sensors. The intent of this section is to give the basic theory and to introduce important parameters used to describe the properties of pixel sensors. This topic is well known in the literature and discussed in several textbooks [1, 2].

Two important parameters strongly related with the conduction of current in silicon are the conductivity σ and the resistivity ρ which can be expressed as follows:

$$\sigma = q\left(\mu_n n + \mu_p p\right) \tag{1.1}$$

$$\rho = \frac{1}{\sigma} = \frac{1}{q\left(\mu_n n + \mu_p p\right)} \tag{1.2}$$

where n and p are the density of electrons and holes, μ_p and μ_n are the mobilities of the two carriers and q is the electron charge. The electron mobility in silicon is 1350 cm^2/Vs and is three times greater than the hole mobility which is 450 cm^2/Vs.

In an intrinsic silicon semiconductor in thermal equilibrium the hole concentration equals the electron concentration and this number is $n_i = 1.45 \times 10^{10}$ cm^{-3}. In this condition, the resistivity of silicon is equal to 3.2×10^2 kΩ·cm. Generally, the intrinsic silicon is not used to develop silicon sensors because it is preferred to modify its with the introduction of impurities (donors and acceptors). The introduction of a concentration N_D of donors increases the n concentration of electrons and in the same way, the introduction of a concentration N_A of acceptors increases the concentration p of holes. When one impurity is dominant, it will determine the resistivity of the semiconductor changing the properties of the whole material. In silicon detectors the substrate resistivity ρ is important to define the depletion voltage of the device and in some cases, it determines the maximum depleted volume.

As it will be discussed in detail in the following sections, conventional MAPS are limited by the charge transportation mechanism in the detector. In order to leave more room for this discussion in the following section, the main two carrier transportation processes in silicon are here introduced. The free carriers can move in the material by drift or by diffusion. When an electrical field E is applied to the material, the free carriers drift following the direction of the electrical field generating in this way a current. The contribution to the total current density given by the transportation of both electrons and holes can be expressed as:

$$J_{drift} = J_n + J_p = q(n\mu_n + p\mu_p)E = \sigma E \tag{1.3}$$

which has been written in the form of the Ohm's Law by using Formula 1.1. By looking at this Formula, one can notice that even if holes and electrons move in opposite directions, they contribute to the total current density with the same polarity. Generally in silicon sensors the electrical field is applied by means of an external bias voltage V_{bias} used to deplete the sensor. In cases where this voltage is significantly greater than the voltage needed to fully deplete the sensor (V_{fd}), the electrical field in the material can be considered constant and equal to $E = V_{bias}/d$.

The second process of charge transportation is generated by the concentration gradients existing in the material. This process, called diffusion, is described by the Fick's Law and its contribution to the total current density in the mono-dimensional case can be expressed as follows:

$$J_{diff} = q\left(D_p\frac{\partial p}{\partial x} + D_n\frac{\partial n}{\partial x}\right) \tag{1.4}$$

where, D is the diffusion coefficient which depends on the mobility and the temperature as expressed by the Einstein relation:

$$D = \left(\frac{kT}{q}\right)\mu \tag{1.5}$$

Considering both drift and diffusion, the current density generated by electrons and holes in the semiconductor is given by:

$$J = J_{drift} + J_{diff} = q\left(n\mu_n + p\mu_p\right)E + q\left(D_p\frac{\partial p}{\partial x} + D_n\frac{\partial n}{\partial x}\right) \tag{1.6}$$

In real applications one of these two mechanisms dominates and it affects important parameters of the device which are important in the field of HEP like the collection time and the radiation tolerance.

1.1.1 The P-N junction

The reverse biased pn-junction configuration depicts the main block used to realize a silicon sensor for ionizing particles. This solution allows to reduce significantly the background generated by the free carriers present in the sensitive volume when no ionizing particles or electromagnetic radiation are crossing the sensor. When new electron-hole pairs are somehow generated in the depleted volume, they can be clearly distinguished from the background of carriers. This condition can not be realized if an intrinsic silicon substrate is used because the number of free carries would be too high to distinguish the induced signal from the background. For instance, in case of a pixel 300 μm thick with an area of 1 cm^2 made by intrinsic silicon, it would contain a background of roughly 10^8 free charge carriers. Since an example of induced signal is of the order of 10^4 free carriers as we will see in this chapter, the signal would be completely lost in the background leading to a not acceptable Signal to Noise Ratio (SNR).

The pn-junction is obtained by the combination of a p-type and a n-type silicon material. The p-region is built by doping an intrinsic semiconductor with a concen-

tration N_A of acceptors while the n-region with a concentration of N_D donors. Close to the junction the majority carriers move by diffusion towards the opposite side of the junction where they can recombine with the majority carriers presents in the new region. As a result of these recombinations, donors and acceptors ions located close to the junction are left without free carriers. Due to this property, this region is known as the *depleted volume* of the sensor and here an electric field is created by the so-called *built-in potential* V_{bi}. The built-in potential prevents the depletion region grow indefinitely.

When the n-region is grounded and a negative external potential V is applied to the p-region, the junction is reverse biased and the depletion volume grows from the interface. The extension of the depleted volume W_{depl} depends on the doping concentrations N_D and N_A, and on the reverse bias voltage applied to the p-region as reported in Formula 1.9.

$$x_n = \sqrt{\frac{2\varepsilon_r\varepsilon_0}{q\,N_D}\left(\frac{N_A}{N_A+N_D}\right)(V_{bi}-V_{bias})} \tag{1.7}$$

$$x_p = \sqrt{\frac{2\varepsilon_r\varepsilon_0}{q\,N_A}\left(\frac{N_D}{N_A+N_D}\right)(V_{bi}-V_{bias})} \tag{1.8}$$

$$W_{depl} = x_n + x_p = \sqrt{\frac{2\varepsilon_r\varepsilon_0}{q}\left(\frac{N_A+N_D}{N_A N_D}\right)\cdot(V_{bi}-V_{bias})} \tag{1.9}$$

where x_p and x_n are the extensions in the p-type and n-type region. Increasing the bias voltage V_{bias}, the extension of the *depleted volume* increases up to fully deplete the device as required to efficiently detect charges generated by crossing ionizing particles. When $N_A \approx N_D$, the depleted volume extends symmetrically on both p and n regions. On the other hand, assuming a junction made by a n-type bulk and a high doped p-type material, the number of acceptors N_A would be higher than the donors N_D and the junctions is called asymmetric. The *depleted volume* in this case extends mainly in the n-region following the Formula 1.10:

$$W_{depl} \approx \sqrt{\frac{2\varepsilon_r\varepsilon_0}{q\,N_D}(V_{bi}-V_{bias})} = \sqrt{2\varepsilon_r\varepsilon_0\,\rho\,\mu\,(V_{bi}-V_{bias})} \tag{1.10}$$

where it has been used the resistivity ρ given by:

$$\rho = \frac{1}{q\mu N_D} \tag{1.11}$$

Formula 1.10 contains the ingredients to obtain large depletions volumes. As it will be discussed in the following, the usage of high resistivity substrates is fundamental to increase the depletion volume. In this equation, the built-in potential V_{bi} can be neglected if considerably high external voltages are applied to the device.

The full depletion V_{fd} is the external voltage which must be applied to fully deplete the sensor. The value of V_{fd} can be found assuming W_{depl} equal to the sensor thickness d in Formula 1.10. The full depletion voltage is given by:

$$V_{fd} = \frac{q\ N_D}{2\ \varepsilon_r \varepsilon_0}\ d^2 \tag{1.12}$$

When an external potential is applied to the diode a current flows through the two terminals of the device. The value of this current is given by Shockley equation reported in Formula 1.13 [1]:

$$J = J_p + J_n = \left(\frac{q\ D_p p_{n0}}{L_p} + \frac{q D_n n_{p0}}{L_n} \right) (e^{qV/KT} - 1) \tag{1.13}$$

where D_p and D_n are the diffusion coefficients of holes and electrons, L_p and L_n are the diffusion lengths, n_{p0} and p_{n0} are the equilibrium electron density on the p-side and the hole density in the n-side, respectively.

When the diode is reverse biased, a small amount of current is generated mainly by the diffusion of free carriers from the undepleted to the depleted region. This current is known as *leakage current* and it is an important device parameter especially if the diode is used as a detector. For the one-side p^+n abrupt junction, $p_{n0} \gg n_{p0}$ and thus the second term of Formula 1.13 can be neglected and the leakage current can be expressed as:

$$J_s = \frac{q D_p p_{n0}}{L_p} \approx q \sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_D} \propto T^{(3+\gamma/2)} e^{-\frac{E_g}{KT}} \tag{1.14}$$

where τ_p is the carrier lifetime, n_i is the intrinsic carrier concentration and γ is a constant. Formula 1.14 gives the maximum leakage current in case of full depletion of the device. For this reason, the measurement of this parameter can be used as a method of estimating the maximum depletion of a real device. Formula 1.14 shows also that the leakage current is strongly dependent on the temperature. By using this relation, it can be assumed that the leakage current doubles every 7 K.

When the bias voltage is further increased, at a certain point the electric field in the depletion volume will eventually reach a critical value generating the *breakdown effect*. In this condition, the free charges in the depleted region are accelerated by the strong electrical field up to reach a sufficient kinetic energy to break the bonds of the silicon lattice thus releasing new free electrons. These new electrons are accelerated as well so that the mechanism is self sustained. Due to this effect, for a critical bias voltage the leakage suddenly increases. If the current reaches very high values the device may be completely damaged. More information about the junction breakdown can be found in [1].

Another important parameter of the reverse biased pn-junction is its capacitance. The depletion-layer capacitance if defined as $C = dQ_c/dV$ where dQ_c is the incremental increase of charge upon and incremental increase of voltage. The capacitance can be calculated assuming the depleted diode as a parallel plate capacitor. The capacitance per unit area before the full depletion can be found using Formula 1.10 as follows:

$$C = \frac{dQ_c}{dV} = \frac{\varepsilon_r \varepsilon_0}{W_{depl}} = \sqrt{\frac{\varepsilon_r \varepsilon_0 \, q \, N_D}{2 \, V_{bias}}} = \sqrt{\frac{\varepsilon_r \varepsilon_0}{2 \mu \rho V_{bias}}} \tag{1.15}$$

whereas when the full depletion is reached ($V_{bias} > V_{fd}$) it becomes a constant value which depends on the total thickness d as shown in the following:

$$C = \frac{\varepsilon_r \varepsilon_0}{d} \tag{1.16}$$

Due to this direct relation between capacitance and depletion extension, the measurement of this parameter is considered another method to study the depletion of the real device. Most of the time, Formula 1.15 is expressed as $1/C^2$ because it makes more evident the capacitance saturation:

$$\frac{1}{C^2} = \frac{2}{\varepsilon_r \varepsilon_0 \, q \, N_D} \, V_{bias} \tag{1.17}$$

A more accurate analysis to calculate the depletion volume extension which takes into account also the majority-carrier contribution leads to the following Formula:

$$\frac{1}{C^2} = \frac{2}{\varepsilon_r \varepsilon_0 \, q \, N_D} \left(V_{bias} + \frac{2K \, T}{q} \right) \tag{1.18}$$

1.1.2 Carrier generation in silicon sensors

Tracking detectors use several sensors since many years to obtain information from the crossing particles. Depending on the application, the information is the position, the released energy or both in order to identify the particle and reconstruct its track. In some applications like the Photon Emission Tomography (PET), also the time information is important.

The signal generated in the detector contains important information about the source who induced the signal. An induced signal in a silicon detector is the result of the generation of free holes and electrons caused by the introduction of electrons coming from the valance band into the conduction band. Considering a reversed bias diode, three main mechanisms can generate the production of these induced pairs: thermal agitation, electromagnetic radiation and ionization by crossing charged particles [2, 3]. It is also possible to inject charges in the device through the forward-biased diode but this condition is not taken into account because the induced signal is lost in the background of charges as already discussed.

The thermal agitation is the main origin of noise in the detector. This contribution indeed, is superimposed onto the signals generated by charged particles or electromagnetic radiation. The thermal excitation is important in those semiconductors where the band gap is small (e.g. Ge) because causes the excitation of several electrons from the valance band to the conduction band. In silicon the energy gap E_g is sufficiently high (1.2 eV) that the probability of direct excitation at room temperature is very low. However, if the crystal presents imperfections, some states may be present in the middle of the gap which increases the probability of thermal excitation.

The carrier generation by means of electromagnetic radiation is the basis of solar cells. In Figure 1.1 is depicted the absorption process for two photon energies. When the absorbed photon has an energy higher than E_g, an electron will move from the valance to one of the empty states of the conduction band. As a result, a free hole is generated the valance band. Electron and hole will then move towards the band

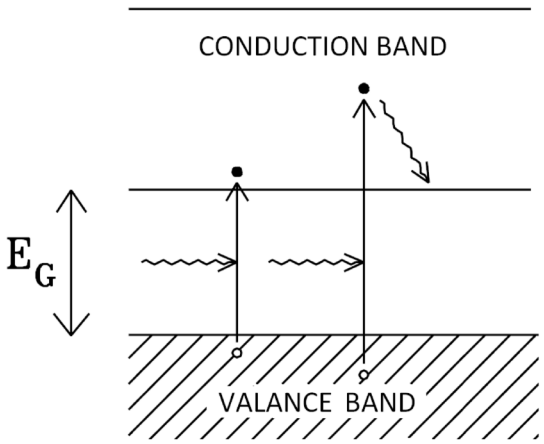


Figure 1.1: *Charge generation by absorption of photons*

gap edges as depicted in Figure 1.1 emitting photons and phonons. If the absorbed photon has an energy lower than E_g, it is not sufficient to generate the free charges. However, the precense of impurities in silicon generates some states in the middle of gap which increases the probability of having charge generation even if $E < E_g$.

The last mechanism of charge generation is due to charged particles moving through the detector. When those particles crosses the sensor, they lose part of their energy through ionization of the atoms of the silicon lattice. The rate of ionization loss of a charged particle in matter is given by the Bethe-Bloch Formula [4]:

$$\frac{dE}{dx} = 2\pi N_0 r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left[ln\left(\frac{2m_e\gamma^2 v^2 W_{MAX}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right] \tag{1.19}$$

where

- $N_0 = 6.022 \times 10^{23}$ mol^{-1} is the Avogadro number
- $r_e = 2.817 \times 10^{-15}$ m is the classic electron radius
- m_e is the electron mass
- ρ is the density of the material
- Z and A are the atomic number and weight of the medium
- z is the charge of a traversing particle

- β=v/c is the velocity in units of speed of light
- δ and C are a density and shell correction
- W_{MAX} is the maximum energy transfer in a single collision
- γ is the Lorentz Factor

An example of application of this formula is shown in Figure 1.2 where is depicted the energy loss of different particles in different materials.

An interesting region of these curves is their minimum which is close to $\beta\gamma \sim 3$. Particles providing such energy loss are known as Minimum Ionizing Particles (MIPs) and they represent a kind of worse-case used to design a detector system because they generate the smallest signal. A good detector should have a noise much below the signal generated by a MIP. In order to understand how important is the SNR, let's make a simple calculation valid for a silicon detector with a thickness of 300 μm and an area A of 1 cm^2. For a proton MIP in silicon the differential energy loss is $\sim$3.87 MeV/cm. Since the mean ionization energy I_0 in silicon is 3.62 eV, the number of free carriers N_{e-h} generated by a MIP particle in such detector will be given by:

$$N_{e-h} = \frac{dE/dx \cdot d}{I_0} = \frac{3.87 \times 10^6 eV/cm \times 0.03\ cm}{3.62\ eV} \simeq 3.2 \times 10^4 \tag{1.20}$$

In order to have a good detector, noise must be below this number.

It is quite interesting to compare this number with the number of carriers in a intrinsic silicon detector with the same volume at T=300 K:

$$N_{intrinsic,e-h} = n_i\ d\ A = 3.87 \times 10^{10} cm^{-3} \times 0.03\ cm \times 1 cm^2 \simeq 4.4 \times 10^8 \tag{1.21}$$

This simple calculation shows again that the signal generated by charged particle is four orders of magnitude smaller than the thermal noise and this explains with more realistic numbers the reason why a reverse-biased pn junction is preferred to build particle detection systems.

The electron and hole pairs generated in the detector by one of the so far described mechanism, after their generation move by drift and diffusion following the direction of the electrical field up to reach the collector node. The time needed to collect the whole signal is known as *collection time* and it is a characteristic parameter of the

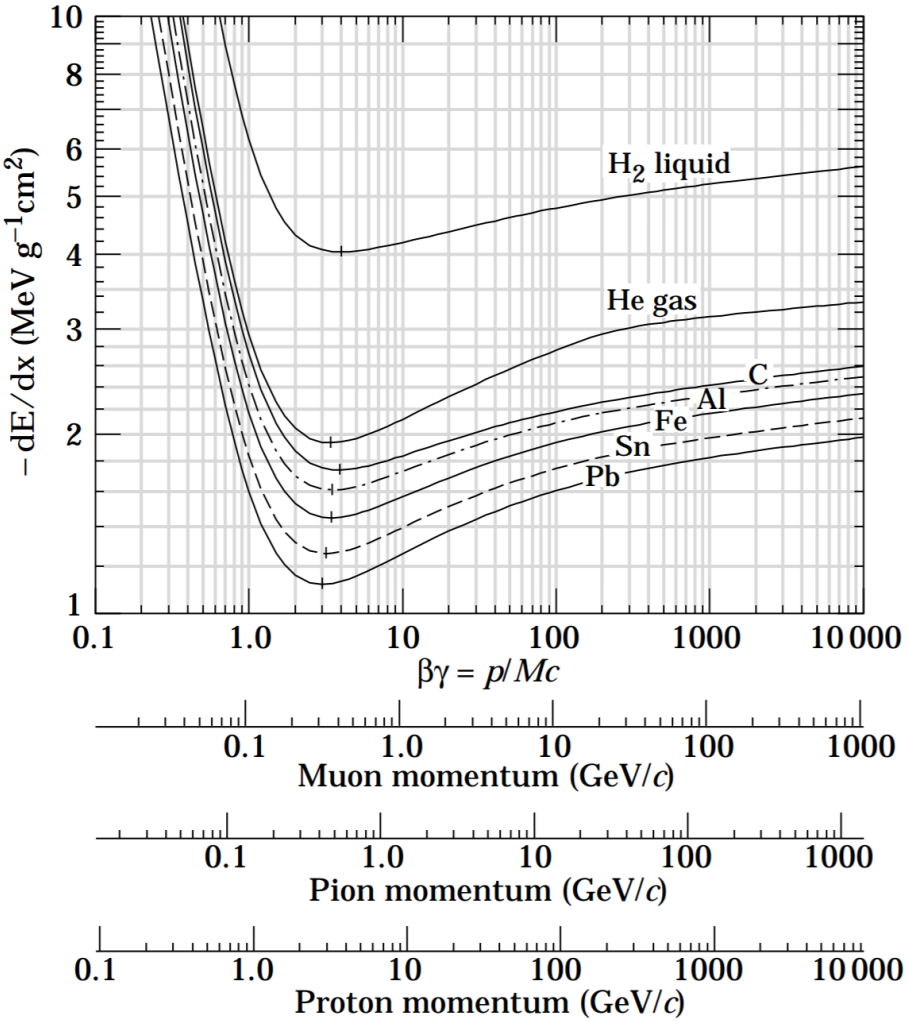


Figure 1.2: *Energy loss of pions, protons and muons in different materials as a function of their energy.*

detector. The free carriers originated by the interaction with the charged particle induce a signal which can be processed by a front-end electronics properly designed to measure time or energy. A very interesting property of the induced signal observed

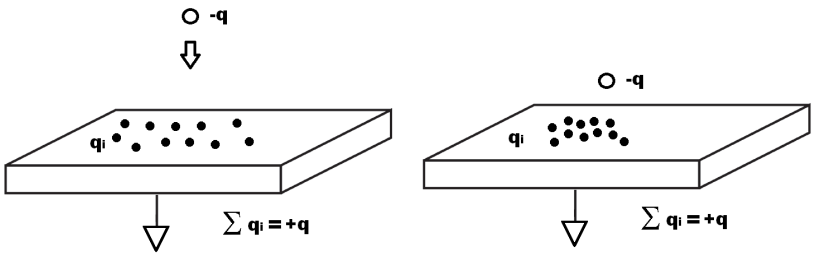


Figure 1.3: *Charge induction in a metal terminal*

by the front-end electronics is that it starts at the same time in which the electron and hole pairs are produced in the detector and not when those charges reach the collector node. This can be explained with the use of the basic electrostatic applied to the situation depicted in Figure 1.3. Here is represented a metal plane connected to ground with a negative charge which floats on the top in two different cases. On the left the charge is far from the surface but it alters the charge distribution in the metal plane inducing a charge equal in magnitude but with opposite polarity. On the right side the negative charge is closer to the electrode and the induced charge is always the same but it has a different distribution. Moving from the first to the second case, the charge distribution on the electrode changes and this generates an electrical current which goes towards the electronics. This process is well described by the Shockley-Ramo theorem and an exhaustive description of the phenomena can be found in [2, 5].

1.2 The monolithic technology

CMOS Monolithic Active Pixels Sensors, known also as MAPS, are silicon detectors commonly used in industrial and medical applications to detect visible light. Due to the several advantages of this technology, those devices are also used to detect charged particles in HEP experiments from the 90s [6–8]. The first scientific use in this field was in 2014 in The PiXeL detector (PXL) of the STAR experiment at the RHIC (Relativistic Heavy Ion Collider) of the Brookhaven National Laboratory to improve the vertex resolution.

The main characteristic of MAPS is the full integration of both sensor and electronics in the same silicon wafer which makes the device very compact. Pixelated sensors realized with this technology can be very small and thus suitable for applications where a good space resolution is needed. In the meanwhile, MAPS allow to reduce the sensor contribution to the quantity of material not used for the radiation detection but where there are undesired energy loss and multiple scattering. This material, known with the name of *material budget*, must be kept the lowest possible to maximize the detection efficiency of the whole detector during the experiments [9]. The monolithic technology allows to overcome in a very elegant way the problem of the interconnection between sensor and electronics. Interconnections for some silicon sensors are a strong limitation because only a few vendors can provide the service with the required precision. This is the case of hybrid active pixels sensors (HAPS). In the hybrid technology, sensor and readout chip are first produced independently and then are physically connected together by means of the bump-bonding technique [10]. The independent fabrication of each part of the device allows the very effective optimization of the properties of both the sensor and electronics making the final device suitable also for applications with extreme environments. For this reason, HAPS are the mainstream in HEP experiments. In Figure 1.4 the structure of a hybrid pixels sensor is depicted. This technology is adopted especially to build the innermost layers of silicon trackers where the particle rate and the total dose are very high. In the case of the High Luminosity Large Hadron Collider (HL-LHC) for instance, the rate close to the interaction point can reach values of 1 GHz/cm^2 and the radiation level can be up to 1 Grad. Table 1.1 shows three experiments where HAPS or MAPS are used. The information contained in the table show that HAPS are used in those environments where the particle fluence is high. This is the case of the innermost pixel detector of ATLAS called Insertable B-Layer (IBL) and the

tracker of ALICE (in case of Pb-Pb collisions) where the values exceed 10^{13} n_{eq}/cm^2. In the case of STAR and ALICE-HL the more relaxed fluence allows to use MAPS taking benefit from the very low material budget. This advantage is clearly visible by looking at the total thickness of the devices. HAPS are always thicker and thus gives more contribution in the material budget. Also in terms of pixel size is clear that MAPS allow the development of very small pixels.

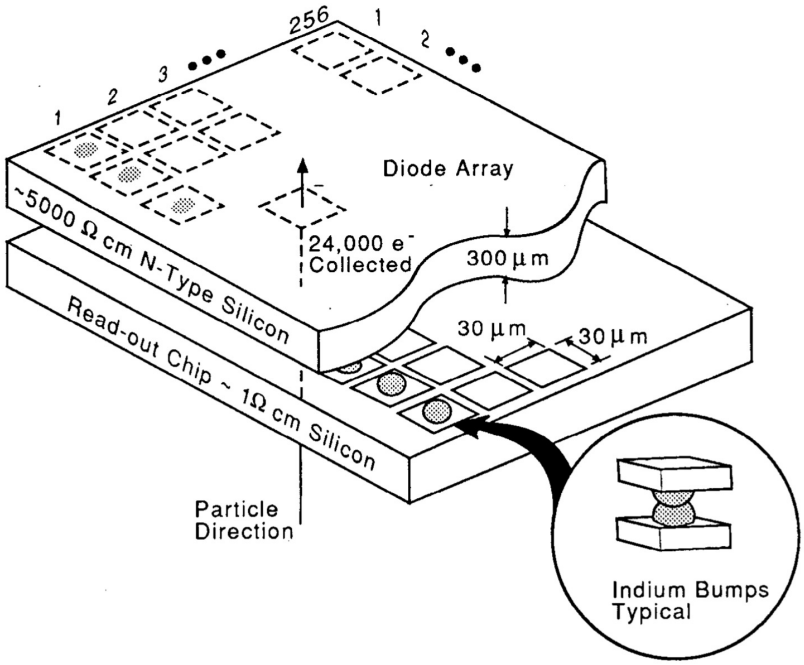
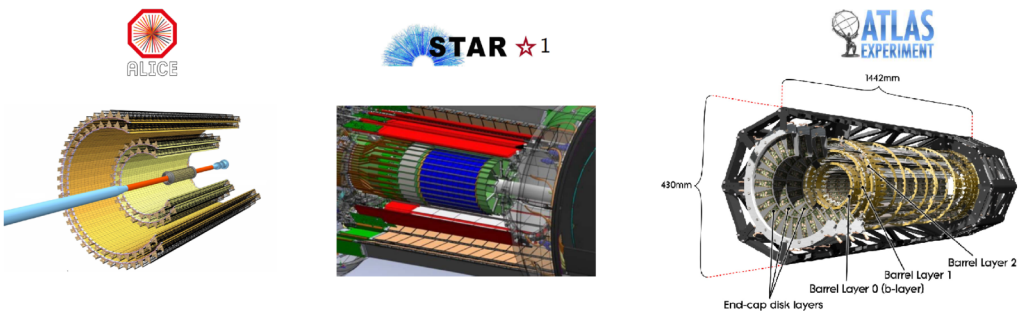


Figure 1.4: *Example of hybrid pixel sensor for particle charge detection [11]*



	UNITS	**ALICE (Pb)**	**ALICE-HL**	**ATLAS**	**STAR**
Bunch crossing	ns	20000	-	25	200000
Particle Rate	kHz/mm^2	15	-	1000	100
Particle Fluence	n_{eq}/cm^2	10^{13}	-	10^{15}	10^{12}
Total Ionizing Dose	Mrad	-	0.7	0.4	0.2
Pixel technology		HAPS	MAPS[1]	HAPS	MAPS
Pixel size	μm^2	50 $\times$ 425	29 $\times$ 27	50 $\times$ 250	21 $\times$ 21
ASIC+sensor thickness	μm	200 + 150	50	200 + 250	50
Material Budget	x/X$_0$	1 %	0.3 %	1.9 %	0.4 %

1- Future upgrade in 2019/2020

Table 1.1: *Three examples of collider experiments where silicon pixel sensors are used*

Even if HAPS have excellent performances, the bump-bonding technique makes these devices quite expensive. The bump-bonding is realized by means of materials like PbSn or In and allows to produce pixels with pitches below 30 μm. Figure 1.5 shows two electron microscope pictures before and after the reflow production step of a PbSn bump with a pitch of 50 μm and diameter of 25 μm [12]. Only a few vendors can realize the interconnections with the fine pitch required by the experiments and as a consequence, the fabrication cost is high. For small projects in particular, this cost and the technical overhead is a strong limitation.

In this context, the monolithic approach allows to overcome this limitation. The fabrication of MAPS indeed merges together the different technologies used for the fabrication of sensor and electronics leading to a considerable cost reduction. This integration is the technological challenge in the fabrication of these devices because the fabrication processing of the two main parts is generally delicate and very different. In the sensor processing, a strong optimization on the wafers is done

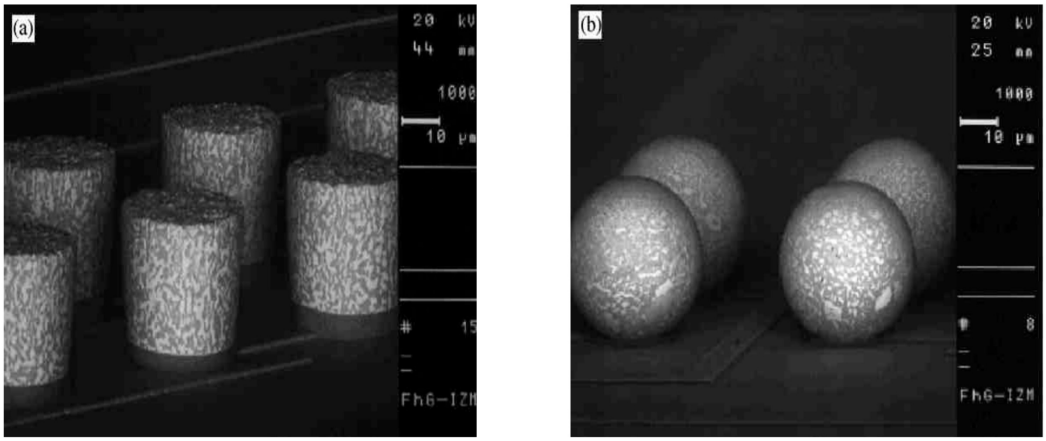


Figure 1.5: *Electron microscope picture of a PbSn bump used to produce hybrid pixel sensors [12]*

to extend the minority carrier life and this is done by using float-zone silicon which is dislocation-free and where the impurities level is very low. In this way, it is possible to fabricate high resistivity wafers. On the contrary, the carriers lifetime in the standard CMOS electronics processing is not important and hence, there are no dedicated optimizations in the substrate material for conserving or improve this parameter. Generally, the substrate of the IC electronics is grown by the Czochralski method. Hence the existence of crystalline defects and impurities makes the carrier life short. In contrast with detectors where the entire substrate thickness is used for the charge generation, IC electronics utilize only a thin layer of few μm on the surface. To guarantee the high quality of transistors this thin layer is lightly doped and have a low defects density. This layer is epitaxially grown on the Czochralski substrate and for this reason is called *epi-layer*. The resistivity of epi-layers is usually among 1-10 Ωcm which is too low than what is required by detectors. As a consequence, sensors made on these wafers would suffer by an early breakdown and maximum depletion limited to few micrometers. Usually the Czochralski substrate is 500 μm and it is used only to provide the mechanical support of the device.

1.2.1 Conventional MAPS

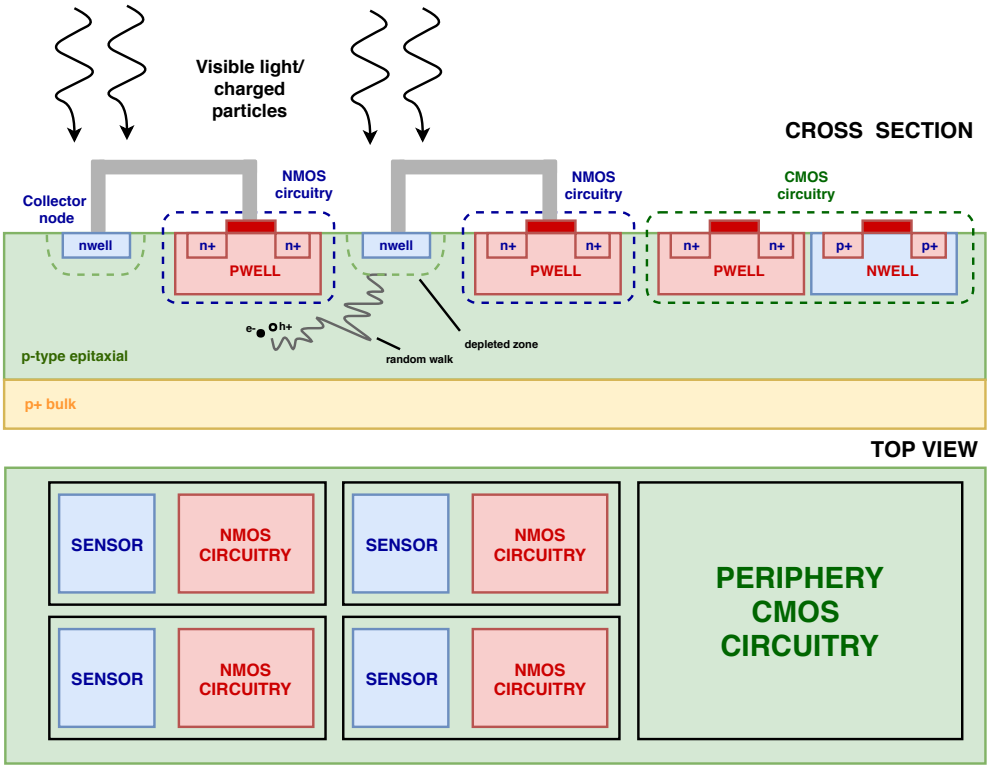


Figure 1.6: *Cross-section (top) and top view (bottom) of a conventional of monolithic sensor.*

The integration of the detector with its readout electronics has always been the most critical issue during the development of MAPS and this led to severe yield problems. In the first generation of MAPS, the ionization volume was implemented by means of thick epitaxial layers and the electronics, based on pure NMOS circuits, was built on it. The cross-section and the top view of a conventional MAPS are depicted in Figure 1.6. The main diode is implemented by the nwell implant used to collect charge and the epi-layer. The diode depletion width depends significantly on the doping levels as expressed in the Formula 1.10. In order to maximize the extension towards the substrate, a low doping concentration and hence a high resistivity wafer is required. Contrary to other sensors used in HEP, the depletion voltage can not be applied to the sensor and as a consequence only the shallow intrinsic depletion is present and it extends for few micrometers from the collector node as shown in Figure 1.6.

In light detection applications, the thin depleted volume below the electronics is insensitive because the light is blocked by the metallization layers of the electronics

and hence penetrates only a short distance. In these applications, the embedded electronics limits the sensitive area of the device and hence, only few transistors are implemented close to the sensor whereas most part of the electronics is placed in the chip periphery. On the contrary, charged particles release energy also in the region below the electronics allowing to reach the 100 % of sensitive area. The free charges generated below the electronics move by diffusion following a random walk path towards the n-well collectors. This collection mechanism is slow and in order to generate reasonable signals it is very important to guarantee a long carries lifetime to avoid the recombination phenomena. Inside of the intrinsic depletion, where it an electrical field is present, charges move by drift but since this volume is much smaller than the whole sensor volume, the charge collection is mainly by diffusion with collection times of electrons in the order of $\sim$100 ns for thin sensors. Albeit in conventional MAPS this has been somehow mitigated by using thick (20-30 μm) epitaxial layers [13], the generated signal is still low ($\sim$1000 e^-).

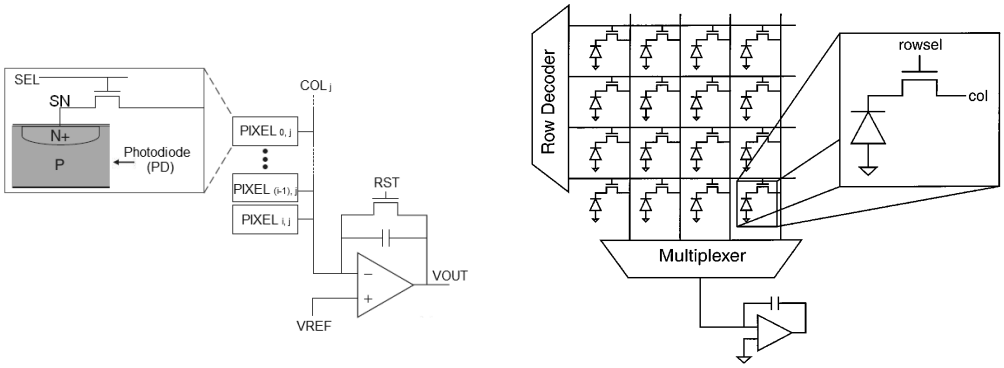
For small pixels sensors this limitation is not dramatic because the sensor capacitance is very small. As a consequence noise is small as well allowing a reasonable overall SNR (around 30). However, noise becomes much higher in case of strips leading to low values of SNR. The slow collection time of these devices makes them unsuitable for applications where time resolution is required.

Also the in-pixel electronics present some limitations. The device in Figure 1.6 shows that the charge is collected by means of the nwell surrounded by the same pwell used to implement NMOS transistors. The usage of additional nwells to implement PMOS transistors would create undesired collectors which would reduce the final charge collection efficiency. For this reason, in the common implant well only NMOS transistors can be used in the pixel area, thus limiting the circuitry complexity at the pixel level. Fortunately, this limitation is not valid for the electronics in the periphery where a more sophisticated circuitry can be placed. In HEP experiments it is also required the usage of radiation tolerant electronics. Conventional MAPS due to their slow charge collection, are vulnerable to bulk damage by non-ionizing radiation. For this reason, the radiation tolerance of these devices is much below the LHC requirements [14]. In spite of these drawbacks, MAPS implementing million of pixels and readout frequencies up to 40 MHz have been produced [4].

1.2.2 Pixel types used in MAPS

In photon detection, the limitation on the single type of transistor available and the reduction of sensitive area led to the implementation of very simple electronics in the pixels. Based on the number of transistors used in the pixel and on the circuitry complexity, the pixel types can be divided in different categories.

- **PPS**: The first implementation is known as Passive Pixel Sensor (PPS) and consists of only one transistor in the pixel which connects the diode to the chip periphery where the signal is amplified [15]. A scheme of this circuitry is given in Figure 1.7a. The advantage of this architecture is the very high



(a) **(b)**

Figure 1.7: *Scheme of a passive pixel sensor on the left and an example of chip with multiplexed pixel selection for the signal amplification.*

achievable fill factor . More architectures can be found based on where the amplification is made. Figure 1.7b shows an example where only one amplifier is used for the entire chip and where the pixel selection is made by means of a row and a column multiplexer [16]. The drawback of this solution are the large capacitive loads made mainly by the long metal lines used to send data to the chip periphery which limits the readout speed.

- **3T pixels**: In this circuit a buffer amplifier is placed in the pixel and for this reason sensors which use this architecture belong to the category of active pixel sensors. The 3T architecture is based on three transistors arranged as shown in Figure 1.8. The incoming signal is integrated on the sensor capacitance which defines the current to voltage gain of the device. One transistor is

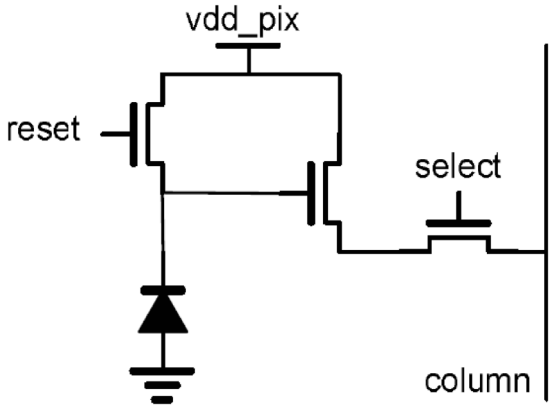
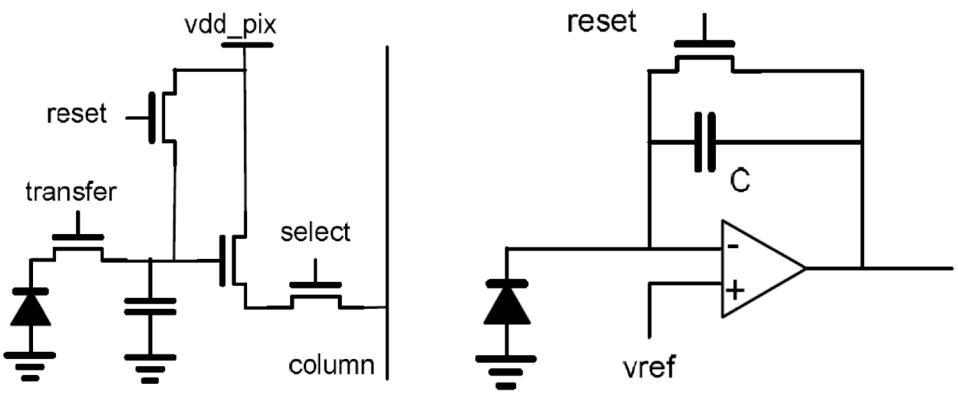


Figure 1.8: *3T active pixel sensor architecture*

used for the reset operation after a readout cycle. The second transistor is the source follower which buffers the signal. The last one is used to connect the pixel to the data transmission bus of the column. A matrix of pixels made with this architecture is readout on a line by line basis. This implies that the integration time between two neighbour rows will be shifted in time, generating a distortion in the data. This readout mode is called rolling shutter and in Figure 1.9 is depicted an example of distortion generated by this effect.

Figure 1.9: *Example of distortion generated by the rolling shutter readout (on the left) and the same picture obtained with a global shutter (on the right)*

- **4T pixels**: This circuit is a modified 3T with an additional transistor and a capacitance used as sample and hold circuit. Figure 1.10a shows how the transistors are arranged in this architecture. The memory element contained in this pixel allows a more flexible readout allowing a distortion-free readout known as global shutter. Thanks to memory element implemented in each pixel, a global signal to start and to close the integration time can be used. When the integration is completed, the information of each pixel is stored in the local memory until the pixel will be selected for the readout. Figure 1.9 shows how the distortion is corrected with this readout mode. The implementation of the capacitance add an additional complexity to the architecture and reduces the fill factor of the sensor.



(a) *4T active pixel sensor architecture* **(b)** *CTIA active pixel sensor architecture*

Figure 1.10: *4T and CTIA pixel sensors*

- **CTIA pixels**: This circuit is based on a Capacitive Trans-Impedance Amplifier (CTIA) with a feedback transistor used for the reset as shown in Figure 1.10b. The conversion gain is therefore defined by the feedback capacitance. This pixel architecture allows a fast readout but due to the implementation of an amplifier in the pixel, the fill factor is smaller compared with the previous solutions [17].

1.2.3 Second generation of MAPS

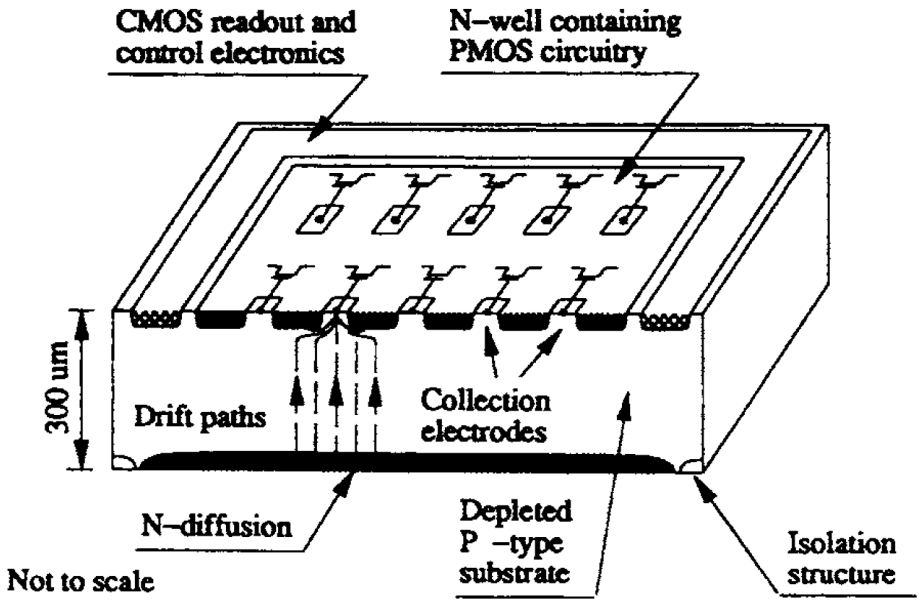


Figure 1.11: *Example of monolithic sensor fabricated with the double-sided processing [18]*

The upgrade of HEP experiments has always been a good motivation to improve the performance of conventional MAPS. In the next generation of experiments, it is foreseen to cover large areas with pixel sensors and cost is becoming a critical factor to take carefully into account. Several R&D activities started to overcome the main limitations of conventional MAPS like the narrow depletion, the low SNR and the low radiation hardness. In order to overcome the limited depletion, several technological solutions have been used to develop the second generation of MAPS during the last years. One of these is the use of the so-called *double-sided processing* which allows to built sensor and electronics in a different wafer side and to insulate them by means of a reverse-biased junction [3]. Figure 1.11 shows the cross-section of a monolithic fabricated by following this approach on a high-resistivity float zone substrate. In this example the sensing volume is made by the asymmetric n^+p junction built at the bottom side which can be fully depleted by means of an external bias applied to the sensor backside. The collector terminals are pwells located on the top and surrounded by a nwell used to built the PMOS electronics of the pixels. At the pixel level, the embedded electronics is made by a pure PMOS first stage amplifier. Then, a further amplification is done in the chip periphery where a full

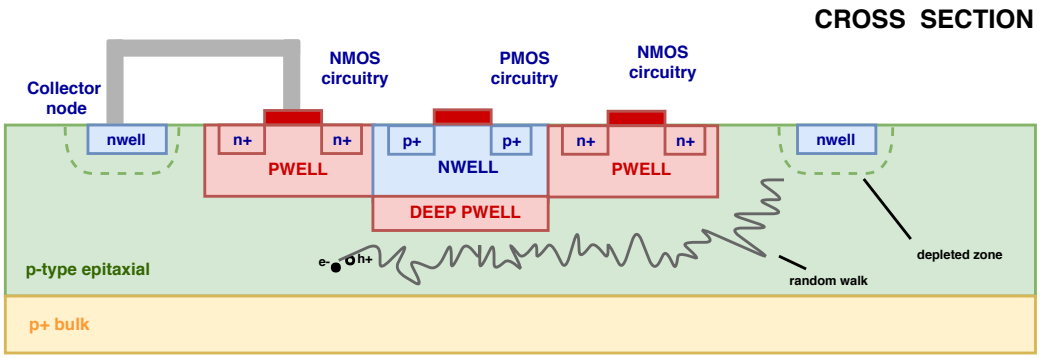


Figure 1.12: *Monolithic sensor with CMOS electronics at the pixel level. Nwells are isolated by dedicated deep-pwells.*

CMOS electronics is built. It has been proved that this approach works [18] and that is is possible to built depleted MAPS, called DMAPS, where the charge is collected by drift. However, the yield of the device was low because of the mechanical damage during the processing and due to the high electric fields under bias.

The limitation of transistor types present in conventional MAPS has been overcome adding an deep pwell implant to isolate the electronics from the charge collection terminals. This solution, depicted in Figure 1.12 allows to implement also PMOS transistors without any charge collection reduction because charge can not be collected by the others since they are shielded by the deep pwell. This approach is used in the ALPIDE chip, the first MAPS which will be used in HEP (ALICE experiment) with sparse readout similar to HAPS. The design concept of this monolithic is depicted in Figure 1.13. The monolithic sensor, developed in 180 nm CMOS

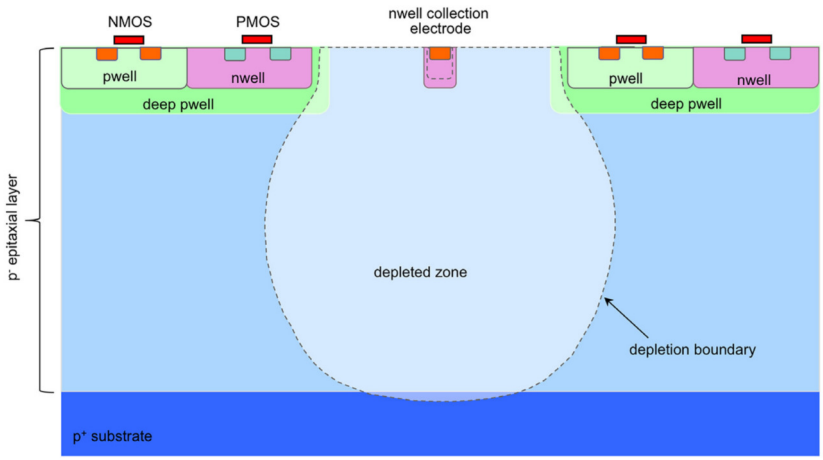


Figure 1.13: *Cross-section of the monolithic sensor used in the ALPIDE chip [19]*

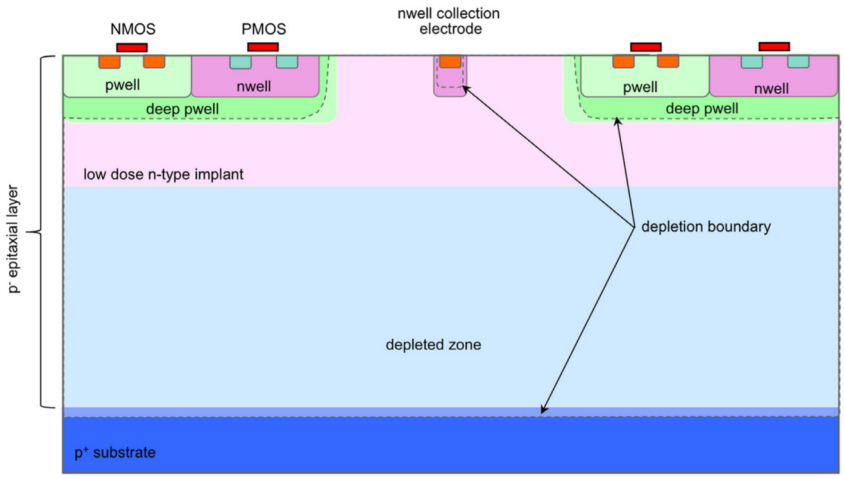


Figure 1.14: *Example of DMAPS developed with a modified process [22]*

technology on a high resistivity (> 1 KΩcm) p-type epitaxial, uses very small collectors which make the sensor capacitance very small (∼5 fF). The region below the collector node can be depleted by using a reverse bias voltage. In such a way, with a voltage of -6 V it is possible to deplete up to 25 μm. This chip is composed by a pixel array of 512 $\times$ 1024 which send data off-chip by means of a sparse readout. In this device, a MIP particle generates 1500 e-h pairs which are collected by drift in less than 10 ns. This makes the device more radiation tolerant than conventional monolithics and reduces the cluster size due to charge sharing between neighbours pixels [19]. However, the region below the deep-pwells is not depleted and this limits the performance of these monolithic sensors. Other examples of devices realized with the deep pwell to isolate electronics and collector node can be found in [20, 21]

The full depletion of the whole sensor volume in a 25 μm thick sensor has been obtained by using a modified process in [22]. In this case the region below the deep pwell can be depleted thanks to the use of an additional n-type layer as shown in Figure 1.14. The main diode in this monolithic is made by the n-type implant and the p^+ epitaxial layer and it is located below the electronics. As a consequence, the depletion starts to grow uniformly among the full sensor up to reach the full depletion of the device. The sensor in this example is 25 μm thick. This solution is a clear example where the full depletion of the device has been reached thus improving the radiation tolerance. A beam test using the 180 GeV/c pion beam at CERN Super Proton Synchrotron (SPS) on a demonstrator chip has proved that with a 10^{15} n_{eq}/cm^2 irradiated sample the efficiency loss is negligible [23]. Based on

this sensor, two large scale demonstrators for the outer layer of ATLAS have been developed: the MALTA and the TJ-Monopix chip. More information about these MAPS can be found in [24]. Another example of DMAPS with a total thickness of 50 μm where a full CMOS circuitry can be used inside the pixel is given by the test chip EPCB01 [25].

In the proposed solutions the full depletion is possible because the sensor thickness is below 50 μm which is enough for several applications. In applications where thicker sensors are required as is for X-rays detection, reach the full depletion is more complicated. In this thesis, a fully depleted 300 μm thick monolithic device is proposed, where the charge collection can be performed by drift and the electronics can be made by using a CMOS electronics.

To complete the description of monolithics, the categories of HV-MAPS and the SOI technology are also described in the following.

1.2.4 HV-MAPS

A separate category of MAPS is known with the name of High Voltage MAPS or simply HV-MAPS. The approach used to increase the depletion of the device consists in built the full circuitry in the collection electrode which acts as a smart diode. In this way a high voltage can be applied to the substrate to deplete the sensor. This allows to reach the full fill factor and in the meanwhile, to provide a high electrical field for the charge collection. Usually a deep nwell is used to shield the low voltage domain from the HV domain as shown in Figure 1.15. MAPS developed with this

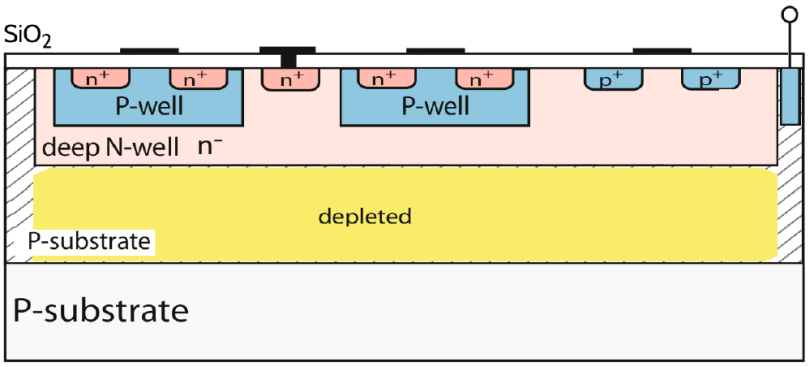


Figure 1.15: *Cross-section of a HV-MAPS*

technology are full/partially depleted and they can use both NMOS and PMOS transistors in the smart diodes. However, since the shield is a deep nwell, PMOS transistors can not be shielded and so, they can be affected by crosstalk through the so-called bulk effect. High voltages can be applied ($\sim$100 V) to the substrate and this allows a fast charge collection which guarantees a good radiation tolerance. It has been observed that HV-MAPS can sustain fluencies higher than 10^{15} n_{eq}/cm^2. The drawback of this technology is the large sensor capacitance (> 100 fF) which affects the noise. Examples and more information about HV-MAPS can be found in [26–29]

1.2.5 The SOI technology

The Silicon On Insultator (SOI) technology, is a new technology tested for the first time by the SUCIMA collaboration [30]. This technology can be seen as the combination of MAPS and HAPS because it aims to take advantages from both technologies. The sensors used in this technology are thick and they are realized with a Buried OXide (BOX) on the surface. The CMOS electronics is fabricated in a separated low resistivity wafer where special cavities are etched towards the bulk. Through these cavities, sensor and CMOS electronics are chemically bonded. Such a device, from the functional point of view, is very similar to the hybrid sensors but it does not need the expensive hybridization to interconnect chip and sensor. Figure 1.16 shows the cross-section of a SOI sensor.

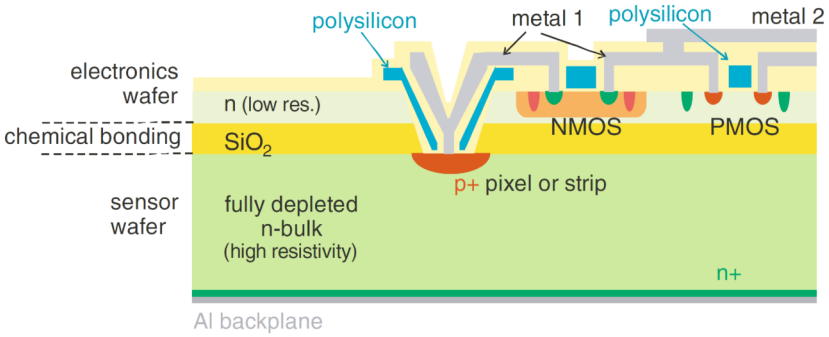


Figure 1.16: *Fully depleted SOI sensors*

Contrary to monolithics, in this technology it is possible to use thick wafers with high resistivity in order to get large depletion volumes. The external bias voltage can be applied to the backside without any risk of affecting the electronics because HV and low voltage domain are separated by the insulator. Usually, thick BOX layers are used to reduce the possible cross-talk between the two domains. Therefore the vertical metal path used to interconnect sensor and electronics must pass through a significant thickness making the reliability of the device an important issue. Proper design techniques, like the use of V-shape cavities allows to overcome this issue [31]. With a proper design both NMOS and PMOS transistors can be used without problems. In some cases, problems have been observed generated by the non ideal Si-SiO_2 interface. Also in this case, they can be avoided with a careful design of the device [3].

The first prototypes of SOI MAPS [32] suffer from radiation damage because charged traps were generated in the oxide layers changing the transistor threshold voltage. An approach used to mitigate this problem consists in using an additional isolation between BOX and electronics making the circuitry more insensitive to radiation effects. With this approach, sensors developed with this technology can sustain fluencies up to 5×10^{14} n_{eq}/cm^2 [33].

Chapter 2

New concept of monolithic sensor

The SEED project (Sensor with Embedded Electronics Development) is one of the ongoing activities of the Istituto Nazionale di Fisica Nucleare (INFN) of Turin. The main goal of the project is the study of innovative solutions for the design of monolithic sensors in commercial CMOS technology with performances equivalent to the ones of hybrid pixels and strips frequently used in HEP experiments. The project would like to prove that the commercial technology can satisfy the very strict requirements of nuclear experiments reducing the manufacturing cost, which is always one of the most important points to take into account. The challenge of the project is of course very ambitious and this can be easily proved after a few studies which highlight the huge limitations of design MAPS without access to the fabrication process data. The collaboration with the industrial partner started on December 2013 and became fundamental to achieve the project goals. The foundry providing the technology allowed to access to the fabrication process data and eventually to customize it with the help of the foundry engineers which shared their experience of several years working with CMOS Image Sensors (CIS). A novel fully depleted monolithic sensor with a thickness of 300 μm has been developed in the SEED collaboration. Two prototypes have been submitted for fabrication in April 2016 with the intention of studying the properties of the novel sensor. The ASICs are 2×2 mm^2 designed in 0.11 μm BSI[1] CMOS technology. The first one is a test chip designed to contain test devices to study the sensor properties. The second is a complete monolithic sensor called MATISSE.

[1] Back-Side Illumination

In this chapter the structure of the proposed sensor developed by the University of Trento is described. Special emphasis is placed on the results obtained during the simulations performed with a dedicated tool named TCAD (Technology Computer Aided Design) from Synopsys. The simulations aims to highlight the limitations of the device with the standard CMOS process. The modified fabrication process is introduced and briefly discussed to describe the new implants added to improve the performances of the sensor. The second part of this chapter is dedicated to the description of the structures implemented in the test chip while the complete monolithic sensor is described in the next chapter.

2.1 The novel sensors of SEED

The proposed sensor aims to overcome the well-known limitations of conventional MAPS with the use of a full depleted thick sensor where the charge collection is performed by drift. The main benefit of this solution is the possibility of collecting the free charges induced in silicon by crossing ionizing particles by drift reducing in the whole sensor volume the probability of recombination of carriers as happens in conventional MAPS. With this solution, together to the possibility of applying higher voltages, it is expected to increase significantly the radiation tolerance of the device .

As discussed in the previous chapter, in traditional monolithics the depleted region is narrow and this limits the amount of charge which reaches the collection terminal. From this point of view, having fully depleted sensors appears the key to enhance the sensor response and hence also to increase the signal to noise ratio of the whole device. A second feature that the novel sensor aims to improve is the radiation tolerance. Is well-known that in silicon sensors, the radiation damage is generated by traversing particles which interact with the atomic lattice through electromagnetic and strong forces. As a result of this interactions, atoms can be displaced creating vacancies or interstitials. These defects generate undesired trap levels in the silicon band gap which reduce the Charge Collection Efficiency (CCE) of the detector [34]. In convention MAPS where the induced charge is mainly collected by diffusion, it has been observed a significant CCE loss due to radiation damage beyond 10^{13} n_{eq}/cm^2 [35]. In the SEED's sensors the charge collection is performed by drift thanks to the usage of electrical fields in the order of tens kV/cm. This will allow a fast charge collection reducing the probability of having trapped charges and thus

improving the radiation tolerance of the device. By using this approach, the novel sensor aims to collect ~ 24 ke$^-$ for a MIP with a SNR of about 400. From the point of view of the radiation damage, a performance similar to what observed in hybrid pixel sensors is expected.

Most of the time, the depletion of large sensor volumes in monolithics is not possible because the devices are not suitable to sustain high voltages or because the substrate resistivity is too low. Furthermore, in several cases where the electronics contains also PMOS transistors, the sensors suffer from low CCE because of the competitive charge collection between the collection electrode and the nwells built to implement PMOS transistors.

The proposed sensor is based on the common p-n junction. The p-region is built by doping an intrinsic semiconductor with a concentration N_A of acceptor impurities while the n-region with a concentration of N_D donors. When the n-region is grounded and a negative voltage V is applied to the p-region, the junction is reverse biased and a depletion volume grows from the interface. The extension of the depleted volume W_{depl} is given by Formula 1.10. The Formula suggests that W_{depl} increases by using high reverse bias voltages V_{bias} and by decreasing N_D as much as possible. Generally this is the reason why high resistivity substrates are preferred to get large depletion regions.

The SEED sensors are based on this kind of asymmetric junction realized with a p^+ implantation made on a high-resistivity n-type substrate with a total thickness of 300 μm. The full depletion of such a thick sensor is a challenge since the required high voltage must coexist with the low voltage CMOS electronics. The proposed solution aims to achieve this goal developing a sensor made by structures placed on both chip sides. This has been possible thanks to the use of the so-called double sided CMOS process. The p^+ implantation is built on the backside together with its metal contact used to provide the reverse bias, while the low voltage electronics is built on the top side. In this way, high voltage and low voltage can be kept separated by reverse biased diodes. Figure 2.1 shows a sketch of the implementation of the proposed sensor where the dashed lines are the representation of the electric field. The p^+ implantation with its metal contact is shown at the bottom. This structure is surrounded by concentric guard-rings realized with small p^+ implantations properly designed to sustain high voltages.

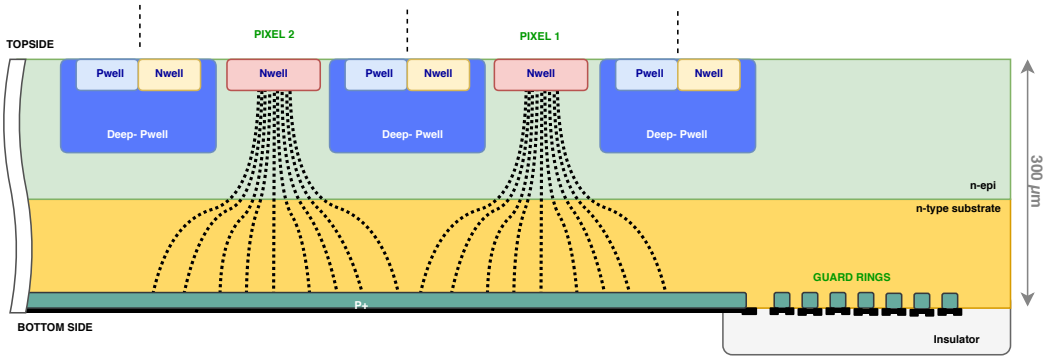


Figure 2.1: *Cross sensor of the proposed sensor*

The chip top side is built with a standard 110 nm CMOS technology with 1.2 V transistors and 6 metal layers. On this side, the charge generated into the depleted volume is collected by a n-well implantation (Figure 2.1). This collection electrode is segmented into an array of small electrodes so that a pixel array is built on the top. The transistors are built inside n-wells and p-wells implanted on a dedicated deep-pwell which shields the n-well from the silicon bulk dividing the high voltage from the low voltage domain. Thanks to this solution, the competitive charge collection is avoided [36]. The deep-pwell is realized into a n-type epitaxial layer used to prevent the punch-through between the deep-pwell and the p^+ when the sensor is depleted. A custom doping concentration profile of this layer has been required to connect the sensor with the electronics without degrading the depletion properties of the device. Although the double-sided technology is required, the production flow of the topside is compatible with the standard CMOS flow.

The use of an asymmetric junction implemented on the backside leads to deplete the sensor from the bottom to the top as depicted in Figure 2.2. As observed for low voltages, the sensor is not fully depleted and free charges are present on the silicon surface which generate resistive paths between different collector. Due to these paths, pixels are not isolated each other and as a consequence a non negligible leakage is injected in all the collectors. The only way to get the electrical isolation of the pixels is the full depletion the whole sensor [37, 38].

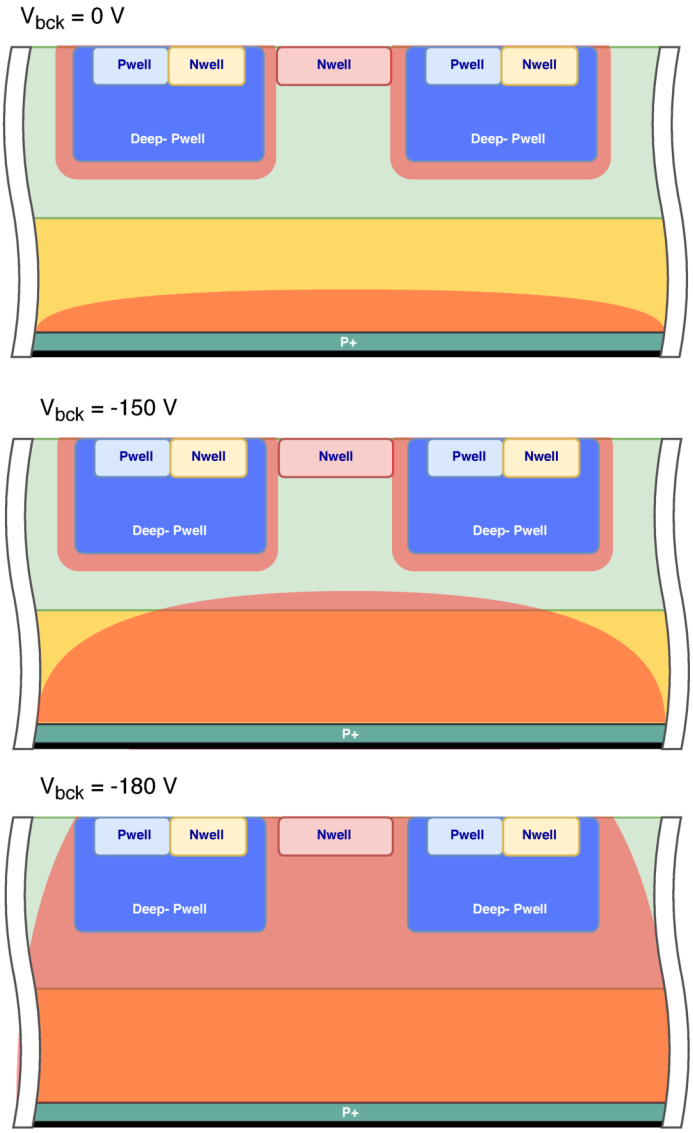


Figure 2.2: *Depletion volume (in orange) with three different reverse bias voltages: 0 V, -150 V and -180 V. The dimensions does not represent the real scale of the sensor.*

2.2 Performance limitations with the traditional CMOS technology

The sensor previously described has been designed with a custom fabrication because the standard process does not to allow to overcome some undesired effects. To study these limitations the structure described in the last section has been simulated in TCAD with the use of the standard process parameters. For the sake of simplicity, the following description focuses on the single pixel but all the concepts can be extended to a matrix of pixels as well. The pixel size used in the simulation is 100 μm $\times$ 100 μm with a collection electrode of 40 μm $\times$ 40 μm located in the middle of the pixel. The silicon substrate is n-type with a low doping realized with phosphorus. This leads to have a high wafer resistivity around $\sim$2 kΩ·cm. The region around the sensing node is dedicated to the electronics, therefore in this area a deep p-well is built. Here are implanted n-wells and p-wells where respectively PMOS and NMOS transistors are built. The top view of the so described pixel is shown in Figure 2.3.

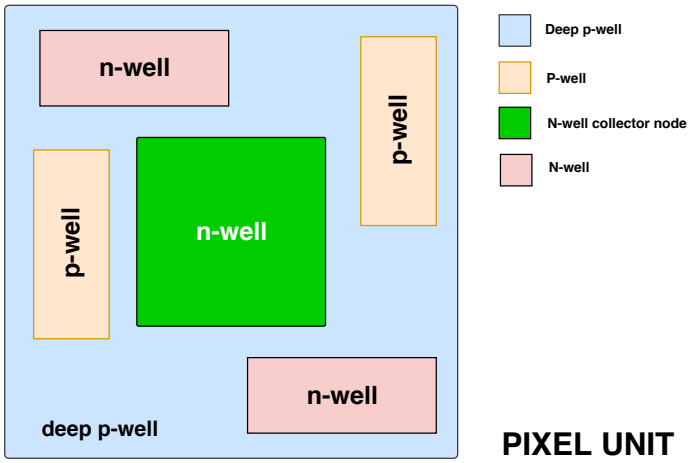


Figure 2.3: *Top view of the pixel unit*

The backside implantation is realized by means of boron dopant with a depth of tens of nm from the backside surface. The cross-section of the device is depicted in Figure 2.4. The properties of the sensor are studied by using the following quantities:

- Full depletion voltage (V_{fd}): defined as the minimum voltage to apply at the backside to get the full depletion.

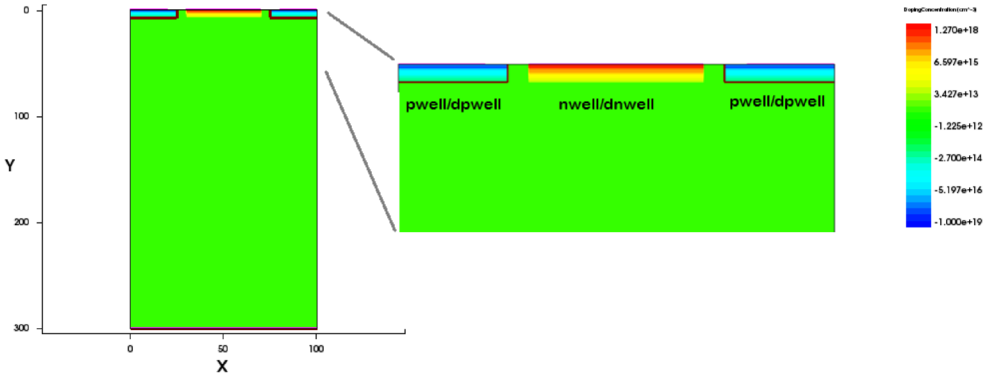


Figure 2.4: *Cross-section of the monolithic device*

- Punch-through voltage (V_{pt}): it is the maximum voltage which can be applied before the increment of the dark current in the diode.
- Capacitance: it is measured between the collection electrode and the back-side contact. This parameter is important for the final noise in the front-end electronics.

The depletion voltage can be studied with a DC sweep of the voltage applied at the backside (V_{BCK}). Figure 2.5 shows the simulated electrostatic potential and the depletion region extension for three different values of V_{BCK}: - 40 V, - 80 V and - 120 V. In this simulation the n-well voltage was set to 10 V whereas the p-wells were maintained at 0 V.

It can observe that at the beginning, when V_{BCK} is 0 V, there is an intrinsic depletion in the front due to the doping concentration of the deep-pwell/nsub junction. When $-V_{BCK}$ increases, a depletion region grows from the backside until it reaches the intrinsic depletion of the front. With V_{BCK} = - 120 V the sensor is fully depleted and thus this value can be considered as the depletion voltage. The maximum electrical field in this condition is around 40 kV/cm. The further increase of $-V_{BCK}$ increases the electrical field allowing a faster charge collection. However, when $-V_{BCK}$ is increased above a certain point the current will increase very rapidly due

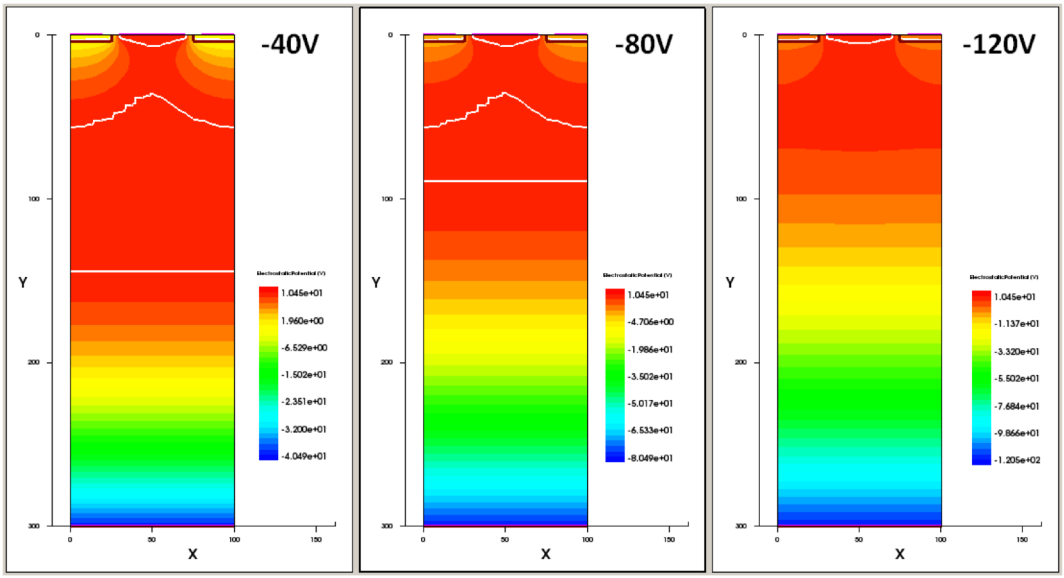
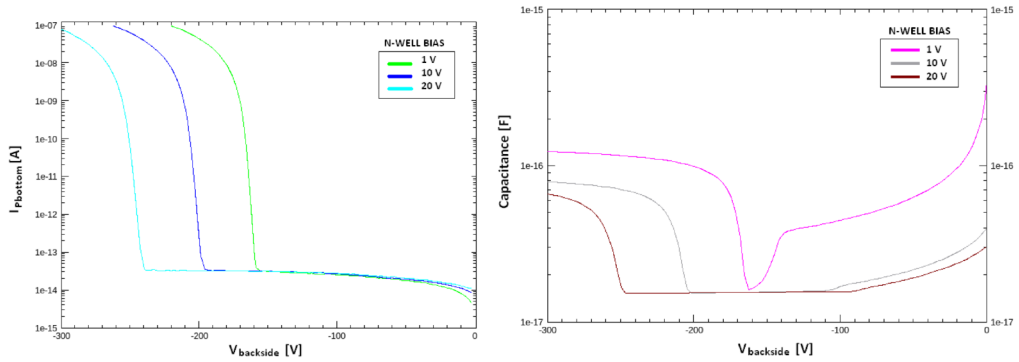


Figure 2.5: *Depletion region extension and electrostatic potential for different values of V_{BCK}: (-40 V, -80 V and -120 V). The white line defines the extension of the depleted volume*



(a) **(b)**

Figure 2.6: *a) I-V characteristic for different nwell bias: 1 V (green), 10 V (blue), 20 V (light blue). b) C-V characteristic for different nwell bias: 1V (pink), 10 V (grey), 20 V (brown). The frequency used for the measurement is 30 kHz.*

to the punch-through. This effect fixes the maximum voltage which can be applied at the backside. Figure 2.6a shows this effect for three different voltages applied to the collector nwell: 1 V, 10 V and 20 V. The current has been measured from the backside node. The highest punch-through is observed around ∼-240 V and is obtained with 20 V . On the contrary, when the voltage bias is set 1 V, the breakdown is observed around -160 V. This result highlights how important is the bias voltage applied to the collection electrode to increase the maximum voltage which can be

applied at the backside. In case of low power CMOS technologies, the maximum allowed voltage is the supply voltage of 1.2 V. Therefore, if the n-well is connected to the electronics through DC coupling, 1.2 V is also the maximum bias which can be used. As a consequence, the breakdown voltage is fixed at low values limiting in this way the maximum electrical field which can be used for the charge collection.

Concerning the sensor capacitance, it is determined by the free charges in the silicon substrate and thus it depends on the voltage applied to the backside by following Formula 1.15. The best way to study its behavior is by means of the classic C-V characteristic obtained with AC simulations. Figure 2.6b shows the characteristic obtained with different bias voltages applied to the collection electrode.

The capacitance is measured between the collection electrode on the top and the pwell on the back. Initially, when the absolute backside voltage starts to increase, the capacitance decreases smoothly until the full depletion is reached. At this point, after the voltage is further increased, the capacitance stays constant at the minimum value until the punch-through voltage is reached. For higher values, the capacitance increases again due to the free holes in the silicon substrate. The three characteristics of Figure 2.6b follow this trend but with different values of V_{fd} and V_{pt} voltages. These values are summarized in Figure 2.7. The difference between these two voltages defines the working region of the device because in this range is possible to fully deplete the sensor and increase the electrical field keeping low the leakage current. For this reason, this region should be large enough for a reliably application. The results show that the higher is the bias voltage applied to the collection electrode, the higher is the working region. In case of setting 1 V to the collection electrode, the working region is too narrow to be reliable. Due to this effect, the proposed sensor designed with the standard fabrication process can not be used for those applications where a DC coupling between the sensing node and the low voltage front-end electronics is required. For those where the AC coupling is possible, the sensor is reliable with bias voltages higher than 10 V and the expected working region is higher than 100 V. During simulations, it has been observed that the punch-through slightly increases if the pixel pitch is reduced as well. However, this variation is too small to be manageable and is not sufficient to increase the working region.

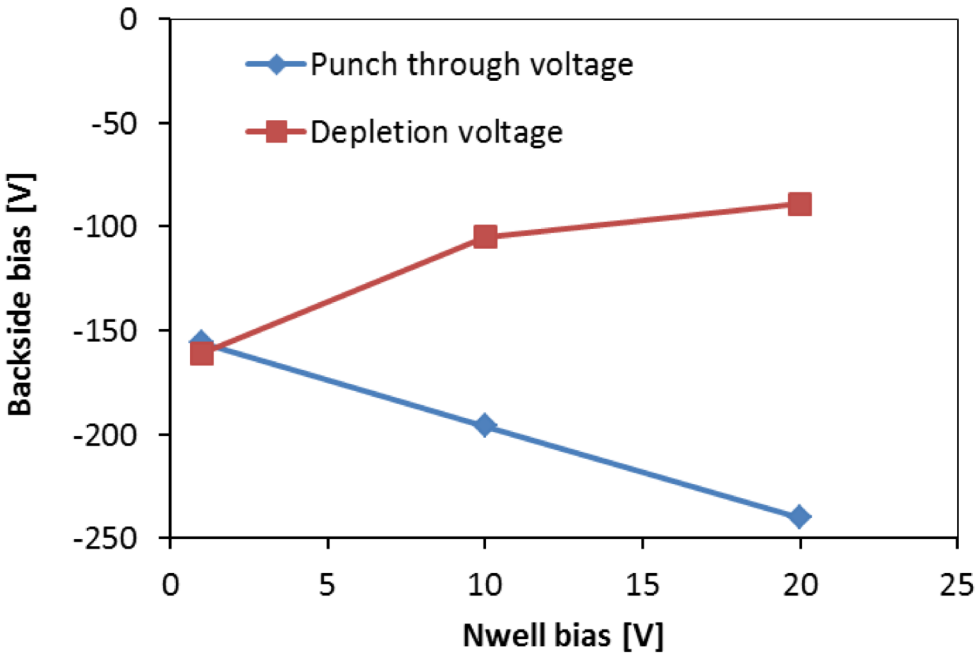


Figure 2.7: *Depletion voltage and punch-through voltage for different nwell bias. All the values are obtained by using the standard process.*

2.3 Custom sensors developed for the SEED project

The main limitation coming from the use of a standard CMOS process is the not sufficient reliability of the device when it is used a DC-coupled readout electronics. A very straightforward solution to increase the working region, and hence increase the reliability, consists of modifying the doping concentration and the depth of the deep-pwell built on the topside. This should allow to move the punch-through voltage towards higher values increasing the final working region. In order to further increase the breakdown voltage is necessary to isolate the deep-pwell by the substrate. This has been realized with the use of a n-type epitaxial layer built on the substrate. The cross-section of the so modified device is shown in Figure 2.1. These modifications require to change the doping concentration profiles used by the foundry and generally this is not possible. However, thanks to the close collaboration with the manufacturer, the custom fabrication has been possible. With these modifications, the punch-through voltage increases allowing to obtain working regions of $\sim$80 V. The total capacitance measured from the collector is dominated by the deep-nwell/deep-pwell capacitance and the expected value is equal 0.8 fF/μm. It can be proved that the optimizations done to increase the punch-through keeping low the capacitance does not have any impact on the sensor depletion.

Table 2.1 resumes the important sensor parameters obtained with the modified process.

PARAMETER	VALUE	UNIT
Nwell voltage	1	V
Depletion voltage	- 160	V
Punch-through voltage	- 240	V
Working region	80	V
Capacitance	0.8	fF/μm
Charge time collection	$<$ 25	ns

Table 2.1: *Important device parameters.*

Figure 2.8 shows the electric potential and the depleted region profile with four different bias voltages in a pixel of 100 μm$\times$100 μm. In this simulation the bias

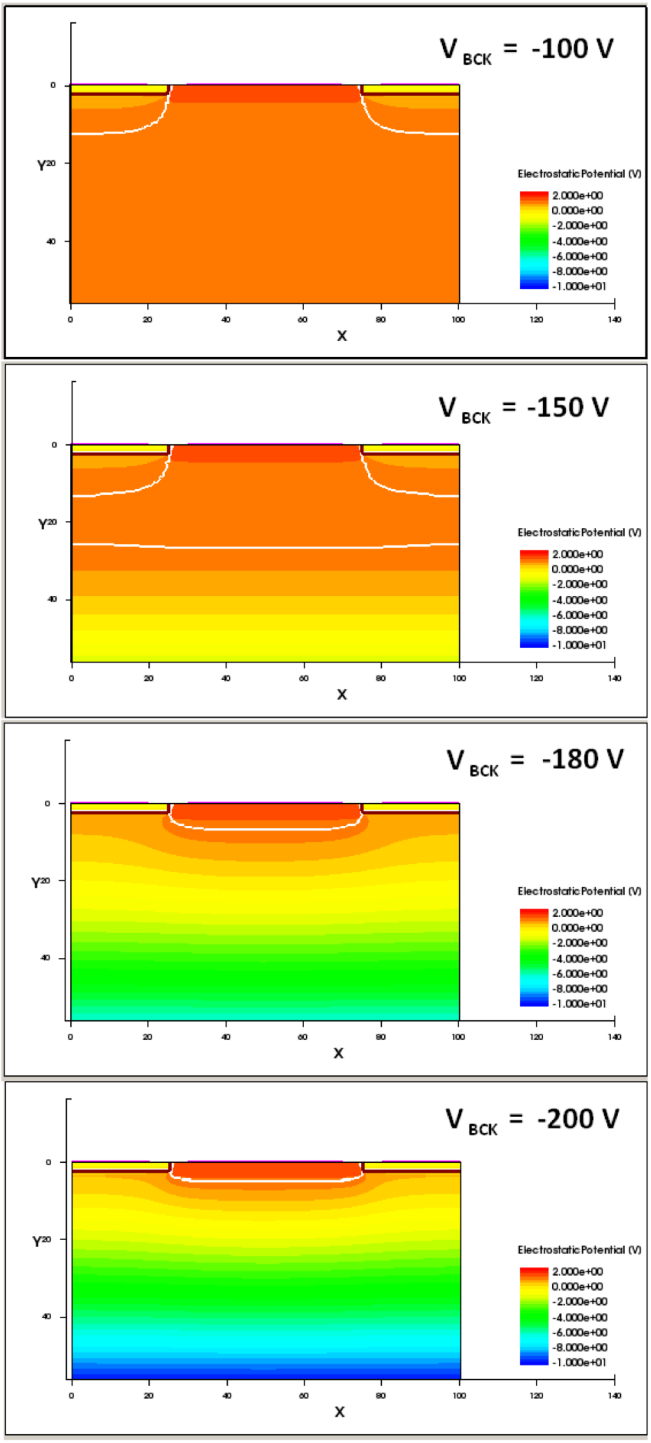


Figure 2.8: *Potential profile and depletion region at the device surface at four different V_{BCK} voltages. The white line indicates the limit of the depletion.*

of the collection electrode is fixed to 1 V and the p-well is grounded. For voltages between 0 and -100 V, an intrinsic depletion under the deep-pwells extends for about 10 μm. When V_{BCK} reaches -150 V, the depletion volume generated from the backside is close to reach the silicon surface. When the voltage is further increased the two depletion volumes merge generating a single depleted volume. The full depletion is expected around -160 V.

As done with the standard process, punch-through and depletion voltage obtained from AC and DC simulations, has been summarized and reported in Figure 2.9. It is shown that with the modified process, also with nwell voltage biases below 1 V, it is possible to obtain large enough working regions. By using this characteristic, a collection electrode bias voltage of 800 mV was chosen. This suggests to use as input transistor a PMOS rather than a NMOS in the in-pixel electronics. With this bias voltage, the full depletion is expected at -165 V and the punch-through around -230 V allowing a good reliability. Moreover, with a backside voltage of -200 V, the complete charge collection (electrons and holes) is expected in ∼25 ns.

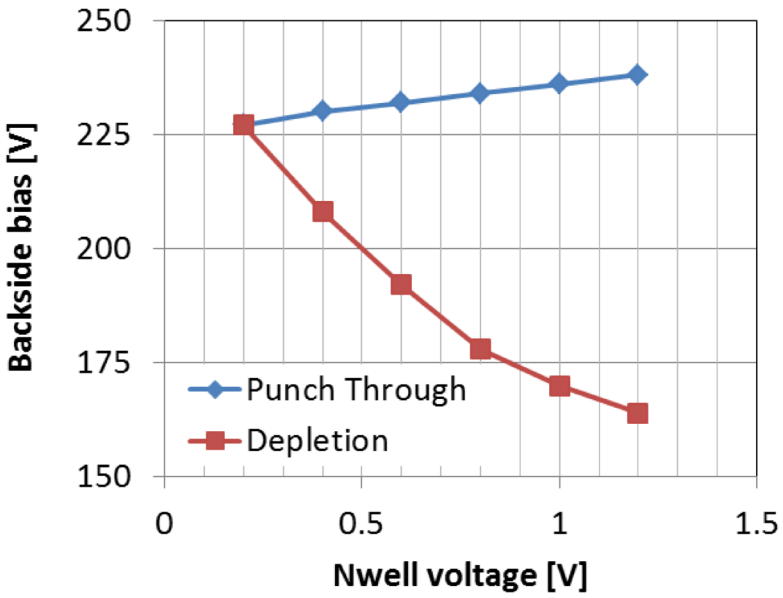


Figure 2.9: *Depletion voltage and punch-through voltage for different nwell bias. Values obtained with the custom process.*

Particular attention has been dedicated to the backside where custom guard-rings have been built in order to obtain the desired performances not foreseen in the standard process.

Based on this sensor, a test chip and a complete monolithic sensor have been produced on custom wafers properly chosen in agreement with the silicon foundry. Three slightly different wafers, identified as wafer 18, 19 and 24 have been used for the fabrication. The wafers have an epitaxial layer with the same charge concentration but slightly different thickness. Also the sensor thickness is slightly different: 300 μm and 290 μm respectively for wafer 18 (24) and 19.

2.4 Test chip description

The concepts explained about the novel sensor have been used to develop a new test chip. The prototype has been designed to contain test devices used to study and quantify the sensor properties in terms of depletion, leakage and radiation tolerance. The structures are kept very simple in order to focus on the phenomena which must be studied. However, even if they are simple, they are built following the same double side process used for the fabrication of the complete monolithic sensor.

The chip design takes into account the planned measurements for each block paying particular attention on the interconnections with the test board. The physical interconnection between the test devices and the test equipment can be made by direct contact with the use of sharp metal needles of a probe station or by wire bonding. In these cases, it is required to mount the prototype so that having the metal pads accessible from the top. A second possible connection consists of using a conductive epoxy glue. This solution can be used when the entire chip side must be electrically connected to the planar metal pad of the test board. The contact so realized is very solid but it is not possible to isolate part of the area from the contact if for some reasons it is needed. The design of the test structures therefore, is closely coupled to the solution adopted to interfacing the test equipment [39]. Based on these considerations, three categories of structures has been selected for the test chip: test diodes, pseudo-matrices and MOS capacitors. They are built on the chip topside or on the bottom-side depending on the planned measurements. The structures have been implemented in a test chip with a die size of 2 mm $\times$ 2 mm designed in 0.11 μm BSI process. Figure 2.10 and 2.11 show both the top and the bottom view of the prototype.

In the backside are visible several diodes with different guard-ring structures used to ensure a homogeneous potential in the whole active area and to shape the field minimizing edge effects. Generally in some devices, the rings are connected to a fixed voltage to collect the leakage currents coming from the edges of the detector. In this test chip, they are left floating to adapt the potential avoiding to have sudden potential drops in the direction of the chip edge. The guard-rings are then isolated by means of a passivation layer which is built at the end of the backside process. Often, in industrial applications this layer is realized with a thin layer of polyimide or pure SiO_2 which can contain several impurities and hence also trapped charge [4]. In those applications where the backside has an active role in the performance of

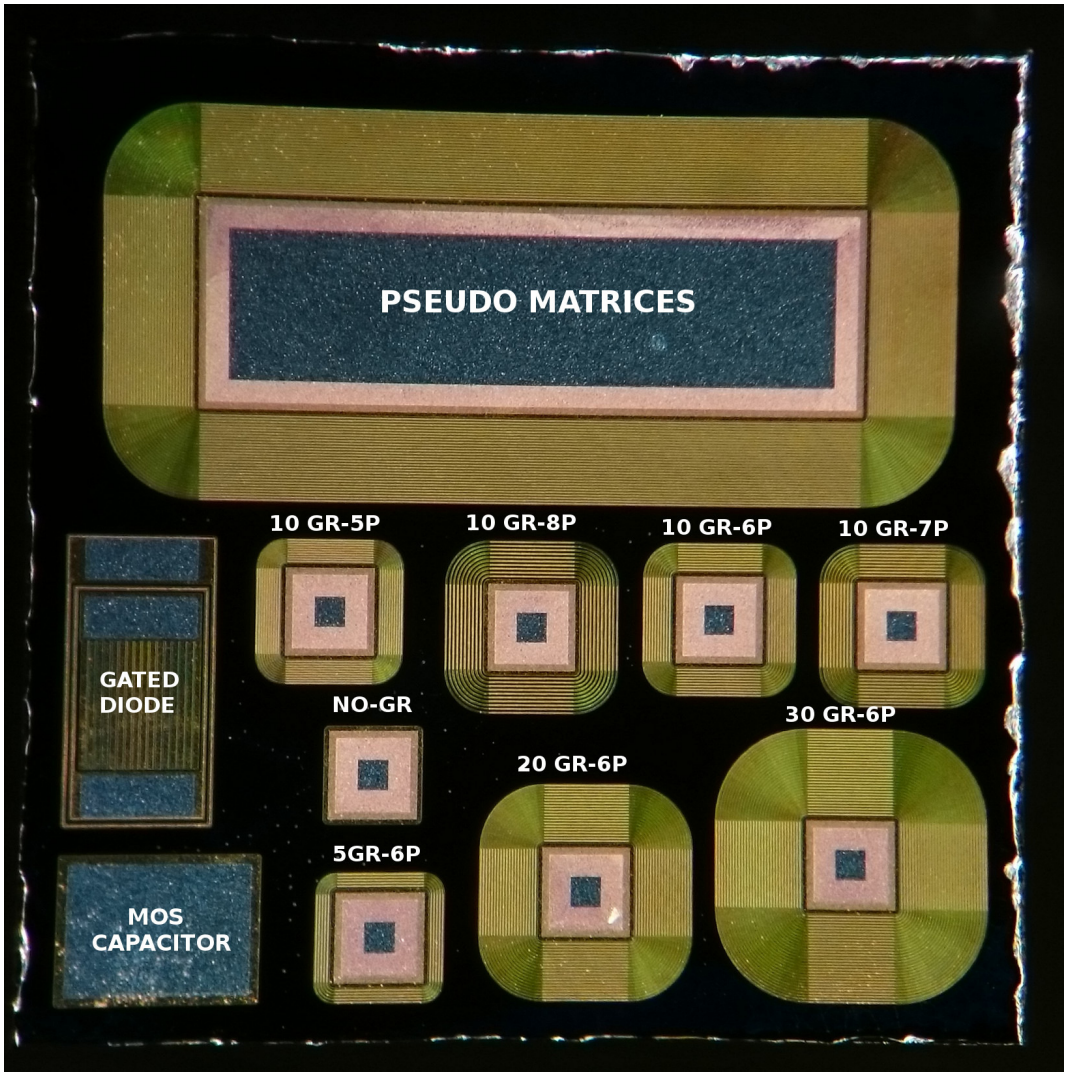


Figure 2.10: *Chip backside: At the top it is visible the big guard-ring(GR) which surrounds the three pseudo matrices. It is composed by 30 rings built with a pitch of 6 µm. At the bottom the eight diodes built with a different number of GRs and different pitch (P) are visible. On the left, close to the chip corner, the structures used for the quality assurance of the backside layers are placed. The white line on the right is the chip edge where are clearly visible some uniformities*

the device, this unwanted charge may alter the properties in the Si/SiO_2 interface and the electrical field of the implants. For example in the case of strips separated by this oxide, the existence of trapped negative charge may lead to the generation of a surface inversion layer which decreases the inter-strip resistance and, is some cases, may generate shorts which can damage the device. Since the guard-rings on the backside are built in the same way of strips, the oxide quality is fundamental to

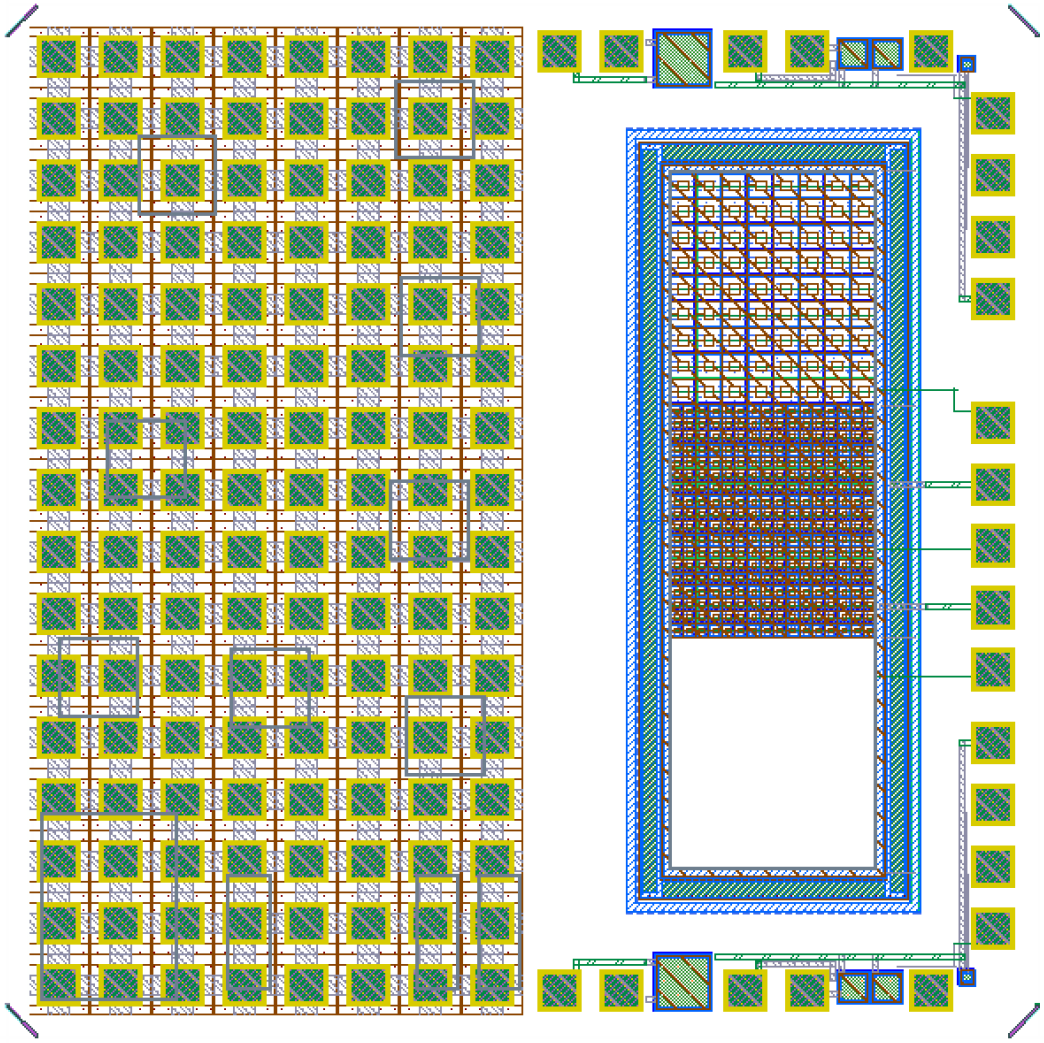


Figure 2.11: *Chip topside. The array of 8 × 16 PADs used for the polarization of the collection electrode is shown on the left. On the right the three pseudo-matrices surrounded by a guard-ring are shown.*

sustain high voltages. The insulator used to build the backside is the commercial Oxide - Nitride - Oxide (ONO) deposited by means of Chemical Vapor Deposition (CVD).

2.4.1 Test diodes

Test diodes aim to study mainly the depletion properties and the behavior of the sensor before and after irradiation. In the novel sensor, the depletion volume grows from the p^+/n-substrate junction realized in the backside and its extension does not depend on the deep-pwell built of the topside. Therefore, the test diodes are made only by the p^+/n-substrate junction. The diodes size is defined by the p^+ implant which is 200 μm $\times$ 200 μm and the polarization of the implant is provided by a metal contact of the same size. Here, the negative high voltage is applied to deplete the sensor. Around the metal contact runs a guard-ring structure used to sustain the high voltage. Generally, the protection effect depends on the number of rings used and on the pitch between the rings. However, since this structure increases the final chip size, one would prefer to get the best protection with the smallest size. Simulations performed in a guard ring made by 10 rings with pitch of 3 and 5 μm show that the small pitch allows to increase significantly the breakdown. The comparison is done taking into account also the possibility of having trapped charge in the oxide used to isolate the rings. Figure 2.13 shows the breakdown voltages obtained in the two cases for three different values of trapped charge in the oxide. Only for high charge concentrations the two structures work similarly. This result proves that the technology allows to make very compact guard-ring thus reducing the final chip size. However, the oxide charge concentration may have a wide variation which can decrease the breakdown voltage degrading the performance of the device.

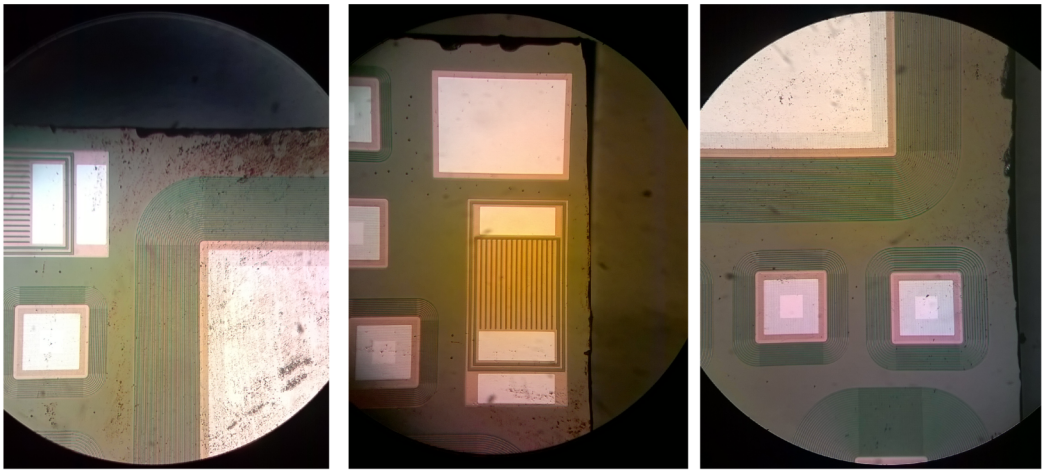


Figure 2.12: *Details of the test diodes implemented on the chip backside. In the figures the metal contacts used to apply the reverse bias voltage and the several guard-rings are visible.*

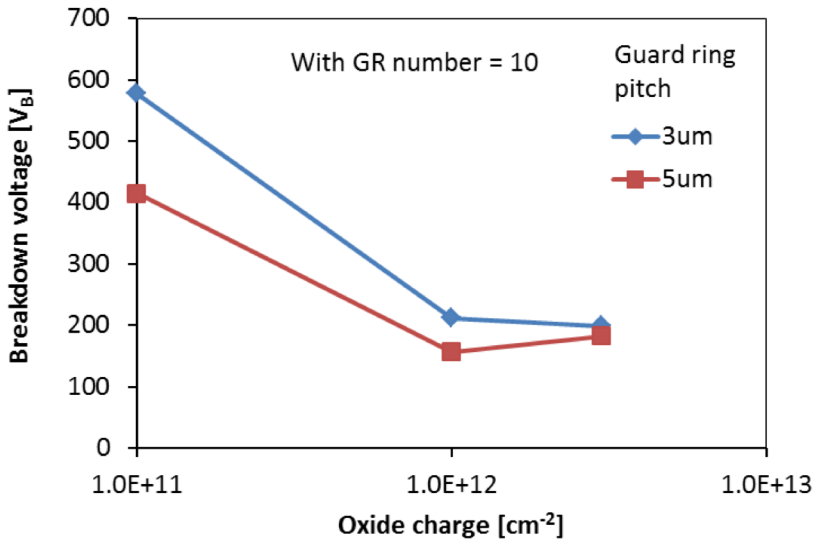


Figure 2.13: *Simulation of the breakdown voltage of two diodes built with guard-ring pitches of 3 and 5 μm*

In order to identify the best trade-off between number of rings and pitch, eight diodes with different protection guard-rings and same size have been built. Those diodes can be grouped into two categories:

- Diodes with pitch of 6 μm: three diodes are designed with this pitch and they use 5, 20 and 30 rings.
- Diodes with 10 rings: they are four and they have a pitch of 5, 6 ,7 and 8 μm.

In addition to these diodes, also one diode without any guard-ring has been built. All these structures can be easily recognized in Figure 2.10. The measurement planned for the diodes are essentially I-V and C-V curves used to study depletion and breakdown voltages. All the measurements can be done providing the reversed bias voltage by means of the metal contact built on the chip back. Each diode has its own contact and thus can be tested independently. For what concerns the topside terminal used for the substrate polarization, it is shared between all the diodes. This terminal has been realized by means of an array of nwells which are well visible on the left side of Figure 2.11. Each nwell has its metal contact for its polarization so, the entire array can be easily connected with the test equipment by means of the conductive epoxy glue.

The cross-section of a typical test diode is sketched in Figure 2.14. Here the p^+ implantation built on the back surrounded by the guard-rings is visible. The picture shows also the passitavion layer used to isolate the rings. On the top the nwell with its metal contact is visible. As observed, the deep-pwell has been not implemented because is not necessary to study the depletion.

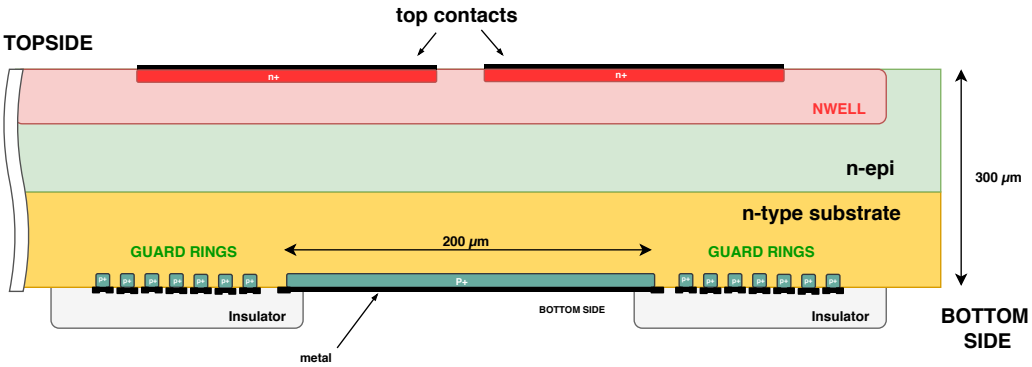


Figure 2.14: *Cross-section of a diode built in the test chip. The guard ring built on the backside of the depicted diode contains 7 rings shielded by an insulator film. The total thickness of the diode is 300 μm and the size is 200 μm $\times$ 200 μm.*

2.4.2 Pseudo-matrices

Three different matrices without electronics are built on the test chip to study the performance of a complete pixel array made by all the custom implantations explained at the beginning of this chapter. Studies on the charge collection time are planned with these test structures. Since, this paremeter depends on the pixel size, each matrix has been designed with different pixel sizes and geometries. The chosen values for the pitches are: 10 μm, 25 μm and 50 μm. Each matrix is 400 μm $\times$ 450 μm and contains a number of pixels which depends on their size. Taking into account these geometries, the three matrices are arranged in 8 $\times$ 9, 16 $\times$ 18 and 40 $\times$ 45 pixels.

Each pixel contains a central region which limits the deep pwell. In this region a octagonal nwell is built to implement the collection electrode. Defining the spacing as the distance between the deep-pwell and the nwell, Table 2.2 resumes the sizes implemented in the three pseudo-matrices.

A cross-section of a matrix is depicted in Figure 2.15. Differently to the diodes, the matrices contain around the collection electrode also the deep-pwell needed to

Spacing [μm]	5	5	3.75
Collector size [μm]	10	5	2.5

Table 2.2: *Collection electrode sizes used in the pseudo-matrices*

built the nwells and pwells for the CMOS electronics. The matrices does not contain transistors but these implantations have been added in order to duplicate the same structures present in MATISSE.

All the collection electrodes are shorted and connected to a PAD. For this reason, the matrices are called *pseudo*-matrices. Around the three arrays, a guard-ring to collect unwanted currents coming from the chip edge has been implemented. This protection ring is realized with a nwell. From the backside, the pseudo-matrices are identical to the diodes but with a different geometry. The p^+ implantation together with the back metal contact are shared between the three matrices and they have a size of 400 μm $\times$ 4350 μm. The implantation is surrounded by a guard-ring made of 30 rings with 6 μm pitch.

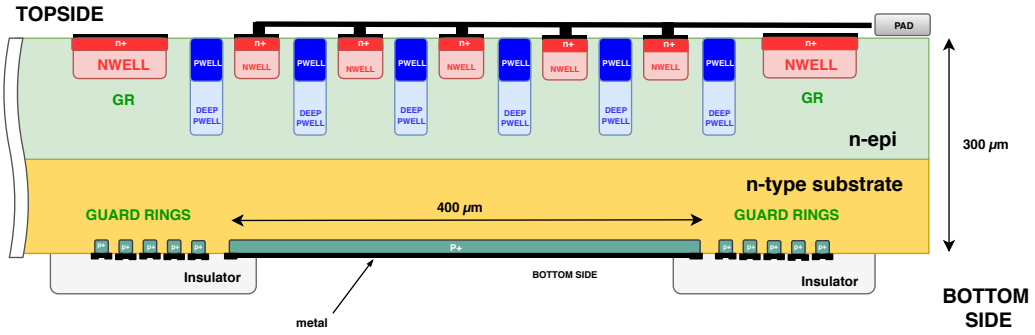


Figure 2.15: *cross-section of a pseudo-matrix built in the test chip*

The three matrices should exhibit different capacitances and so they can be used to study the dependence of the capacitance from the collector perimeter. In general, the smaller is the collection electrode, the smaller is also the capacitance. In addition to the capacitance measurements, these structures can be used with an external fast amplifier to measure the charge collection time.

2.4.3 MOS capacitors

The fabrication of the oxide layer in CMOS technologies is always a crucial step. For this reason, its quality must be accurately verified. However, the verification of the layers built on the backside process is not a quality assurance (QA) item for the manufacturer and so it must be done with a proper diagnostic tool as it is the MOSCAP device. This device is realized by using the same oxide insulator built to protect the guard-rings and thus, it can be used to study important parameters of the insulator like the oxide thickness, the trapped charge in the oxide, the doping concentration of the p^+ implant and the interface trap densities. All these parameters can be obtained by means of the capacitance-voltage technique.

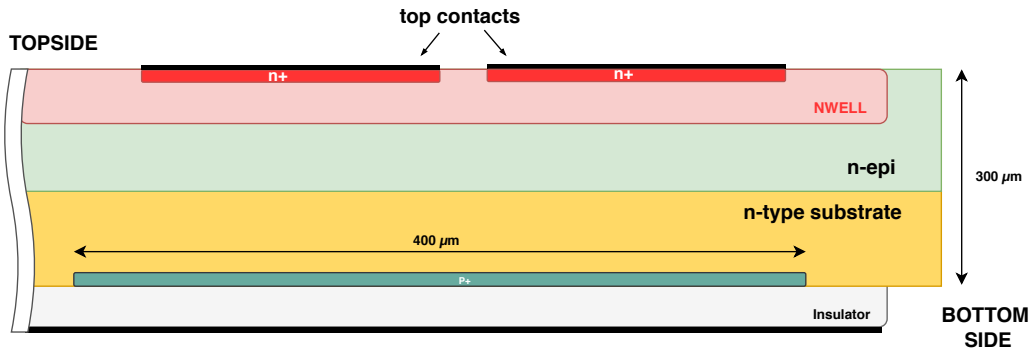


Figure 2.16: *Cross-section of the MOSCAP built on the test chip for the quality assurance of the backside*

The MOSCAP built in the test chip is 300 μm $\times$ 300 μm. A cross-section of the device is shown in Figure 2.16. On the topside, it shares with the diodes the top electrodes used for the bulk polarization. Therefore, all the measurements on this capacitor can be done placing the sample bottom up and connecting the top face by means of wire bonding. On the backside, the MOSCAP is made by a structure composed of a p^+ implantation, the ONO insulator and the metal contact.

Chapter 3

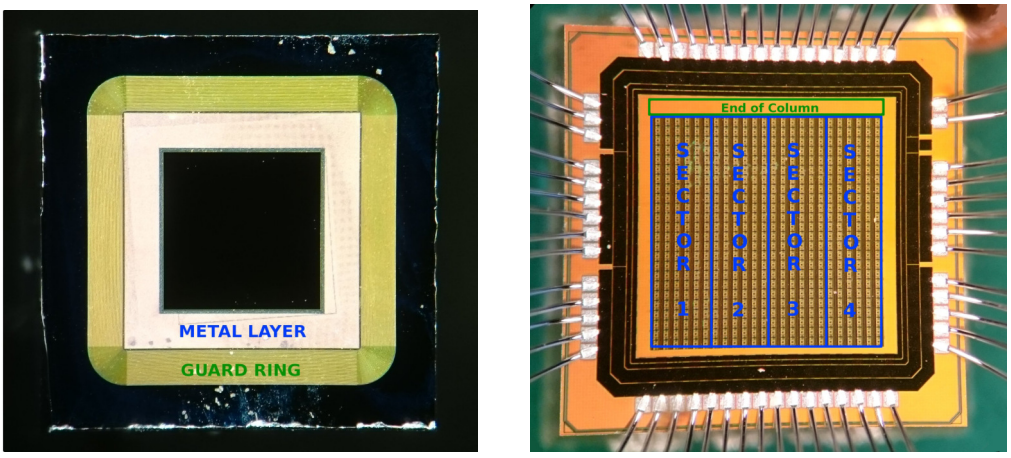
The MATISSE chip

MATISSE (Monolithic AcTIve pixel SenSor Electronics) is a monolithic sensor of 2 mm $\times$ 2 mm based on the novel fully depleted sensor previously described connected with a dedicated embedded readout electronics. The main target for this ASIC is the integration of an analog readout able to take the weak signal coming from the sensor and to generate an enhanced one which can be sent to the external world. In such a way, the circuitry makes possible to deeply study the sensor, quantifying its performance and, in the meanwhile, to use the complete monolithic sensor to detect radiation.

In the first part of this chapter, the sensor of MATISSE is described highlighting the differences introduced from the sensors built on the test structures. The sensor is shown in detail with the description of the structures built on both chip-sides. The second part is dedicated to describe the integrated electronics used in the matrices. The top level logic of the ASIC is shown by means of the description of the block which manages most part of the chip logic: the End of Column. The in-pixel electronics, both analog and digital, is described with the analysis of the architectures used to build the front-end together with the design techniques used to meet the specifications such as low noise and high dynamic range. At the end, the possible readout operations, like correlated double sampling and double sampling, are shown with particular attention to the effect of noise which is fundamental in applications where the most important information is the energy resolution as happens in X and gamma-ray spectroscopy.

3.1 Sensor description

MATISSE has been fabricated using a n-type high-resistivity substrate with a thickness of 300 μm. The sensor production has been divided into two main steps: first, the topside has been built with the commercial 0.11 μm CMOS process flow and then, all the required structures to deplete the sensor have been built on the backside. Such structures are the same used in the test diodes and matrices but with different geometries to fit the dimension of the pixel array of the chip. Therefore, on the detector backside, a p^+ layer has been implanted with its metal contact surrounded by guard-rings required to sustain high voltages. The p+ implantation area is 1.25 mm $\times$ 1.25 mm and defines the active area of the sensor. It is polarized by means of a square annulus metal contact of 1.23 mm $\times$ 1.23 mm. The area in the middle is 0.85 mm $\times$ 0.85 mm and is kept metal free in order to be able to test the sensor also with a laser minimizing the scattering with the metal layers. For this purpose, a glass opening has been used. The guard-rings which surround the metal layer consist of 30 concentric rings of 3 μm width organized with a pitch of 6 μm. The guard-rings are protected by an oxide layer in order to be able to contact the p^+ by using an epoxy glue which covers all the backside. A sketch of the backside is depicted in Figure 3.1a.



(a) **(b)**

Figure 3.1: *Backside (a) and topside (b) view of MATISSE*

The topside of MATISSE contains a matrix array of 576 pixels implemented in an area of 1.2 mm $\times$ 1.2 mm. Each pixel is 50 μm$\times$50 μm and contains a collection

electrode of 20 μm $\times$ 20 μm located in the middle. The collection electrode is a nwell used to collect the charge generated in the bulk. As already described in chapter 2, the biggest contribution to the sensor capacitance comes from the collector node perimeter. This capacitance plays an important role in the final signal to noise ratio of the device because it determines the value of the 1/f term [40]. In order to find the best dimension and shape which minimize the electronic noise, MATISSE has been designed by using eight different topologies of collectors. Figure 3.2 summarizes the topologies used in the prototypes.

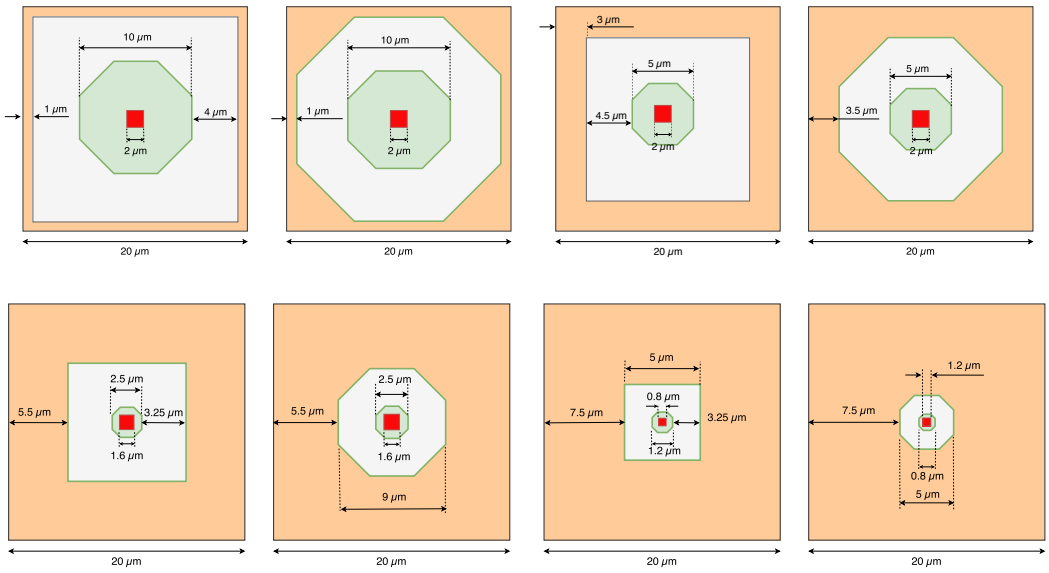


Figure 3.2: *Different geometries used for the collector node. Each square is 20 µm×20 µm. The n^+ is depicted in red with its metal contact, in green the nwell and in orange the deep-pwell*

The matrix array has been logically arranged in four independent regions called sectors. Sectors are identical from the point of view of the embedded electronics, but they differ by the collector node topology used in the pixels. In order to implement the eight topologies, two different flavors of MATISSE has been produced. Figure 3.1b shows the chip topside with the matrix arranged in sectors.

Each pixel of MATISSE embeds a circuitry for the signal processing implemented on nwells and pwells built on a deep-pwell which surrounds the collection electrode as shown in Figure 3.2. Figure 3.3 shows the cross section of the prototype.

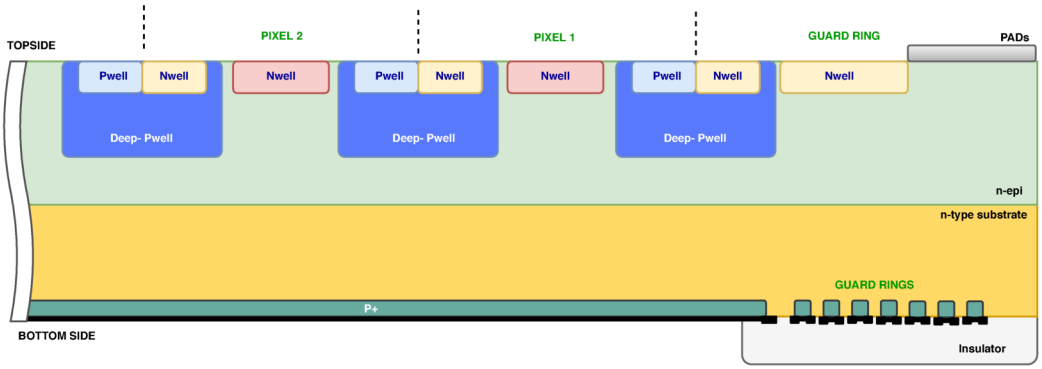


Figure 3.3: *Cross section of MATISSE. At the bottom are shown the guard-rings and the metal contact used for the polarization of the diode. At the top, the pixel array built on nwells and pwells. Between the first pixel and the PAD is shown the guard-ring built on the top used to protect the pixel array from undesired currents.*

Even if MATISSE is a 2 mm $\times$ 2 mm chip, the active area of the sensor is defined by the geometry of the backside and in particular by the p^+ implantation which is 1.25 mm $\times$ 1.25 mm. The small distance between the edges of the depletion region and the cut line of the silicon die can lead to a non-negligible contribution from the leakage current originating in the highly defective lateral surface of the chip. In order to collect this unwanted current, a biased guard-ring realized by means of a nwell implant has been built around the pixel matrix [41]. The bias of this protection can be tuned because is connected to a PAD. This guard-ring is visible in the layout of the chip corner shown in Figure 3.4.

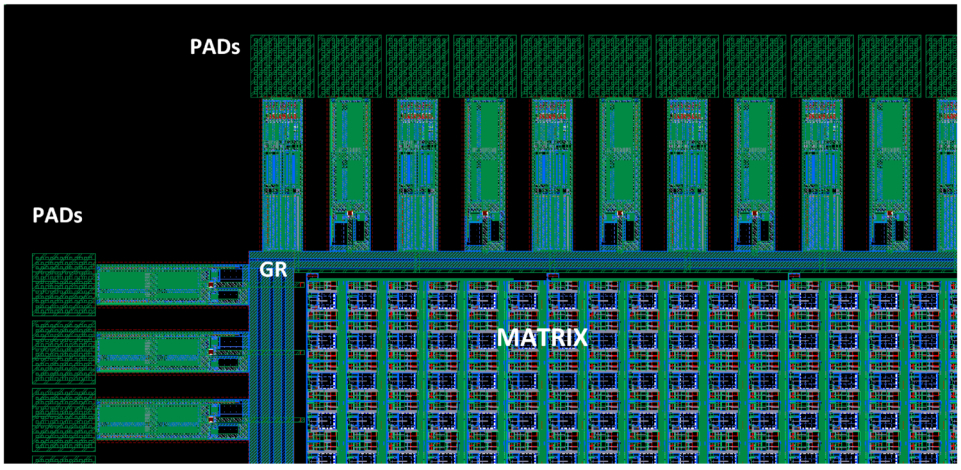


Figure 3.4: *Layout of one corner of MATISSE. The guard-ring protection is built between the matrix array, located on the right side, and the PADs*

As one can observe in the Figure, the guard-ring has been kept separated by the chip border in order to collect as much as possible the undesired lateral currents which can significantly affect the sensor performance [41].

3.2 The embedded electronics

MATISSE has been developed in a commercial 0.11 μm CMOS technology with 1.2 V transistors and six metal layers. Each prototype contains 59 pads of 74 μm$\times$74 μm each, distributed on the four sides of the chip. In order to have a very effective control of the prototypes, the polarization of the bias cells is provided by SMD resistors located on the carrier board used for testing. Therefore, most of the PADs are used to send voltages and currents needed to the readout circuitry. The embedded electronics is implemented on the top side by following the conventional CMOS flow. The 576 pixels are arranged in a matrix of 24 $\times$ 24. As already introduced, the matrix is divided in four sub-matrices: each one contains six column of 24 pixels. Pixels of the same column share two data transmission lines to send data off-chip allowing to significantly reduce the metal density along the columns. The twelve data buses of each sector are then merged in two main buses connected to dedicated PADs. Therefore, MATISSE has in total eight analog outputs properly buffered.

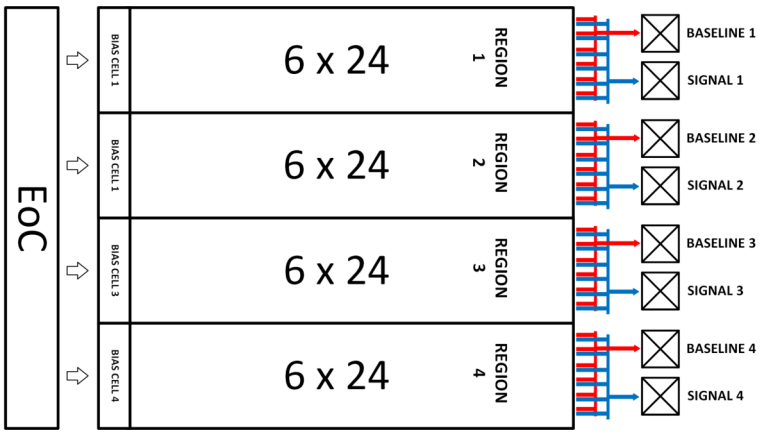


Figure 3.5: *Main blocks of MATISSE: the matrix array is divided in four sectors of 6$\times$24 pixels. The entire logic is managed by the EoC*

The entire logic of the columns is managed by an End of Column (EoC) block located close the first pixels of the column. This block is used to set the configuration of the whole matrix and to manage the communication between channels and external

world. Thanks to EoC logic, the sectors can work in parallel. To provide a reference for the following description we will define that the EoC is located at the bottom of the matrix. Following this reference, the pixels are numbered starting by the EoC from 0 to 23 whereas the columns from 0 to 23 from left to right. Figure 3.5 shows a schematic representation of the main blocks of MATISSE.

The embedded electronics of the single channel plays a key role in the readout chain of the device. The whole information associated with an event indeed is processed at this level by keeping the signal degradation as low as possible. For this reason, low degradation is one of the most important requirements which the embedded electronics must satisfy. Not less important is the maximum silicon area which can be used for the circuit. In principle, one can decide to implement sophisticated circuits to minimize the information loss but in most of the cases, this implies the use of very large areas of silicon usually unavailable. In the case of detectors for particle physics, for instance, space is a crucial information to develop the integrated "eyes" used to detect particles. In fact, when pixel silicon sensors are employed, the smaller is pixel size the better is the final spatial resolution which can be achieved [4]. Taking into account those considerations, the pixel size chosen for the matrices is 50 μm $\times$ 50 μm, shared between the sensor and the electronics. As already introduced, a square of 20 μm $\times$ 20 μm located in the middle of the pixel is dedicated to the collection electrode whereas the remaining area (84 % of the pixel) is dedicated to implement the in-pixel electronics. 64 % of this space is used for to implement the analog circuitry and the remaining 36 % for the in-pixel digital logic. In order to block eventual digital noise injection in the analog front-end, the two domains have been kept physically separated as shown in the block representation in Figure 3.6

The target for this first version of MATISSE is measuring both energy loss and the hit coordinates. The expected charge for a MIP particle in the condition of full depletion exceeds 24 ke$^-$ which are collected in $\sim$25 ns. Charge is estimated by measuring the voltage amplitudes therefore, the implemented electronics must be able to cover the full range of charge allowing a linear response and a low noise. The target for MATISSE in terms of noise is 100 e$^-$. The eight sensor flavors with slightly different capacitances can be used to identify the optimal solution to increase the signal to noise ratio of the device. The pixel matrix is readout by means of snapshot shutter thanks to the use of two local memories in each pixel. Speed is not a goal for this version, thus it has been possible relaxing the specifications of both the

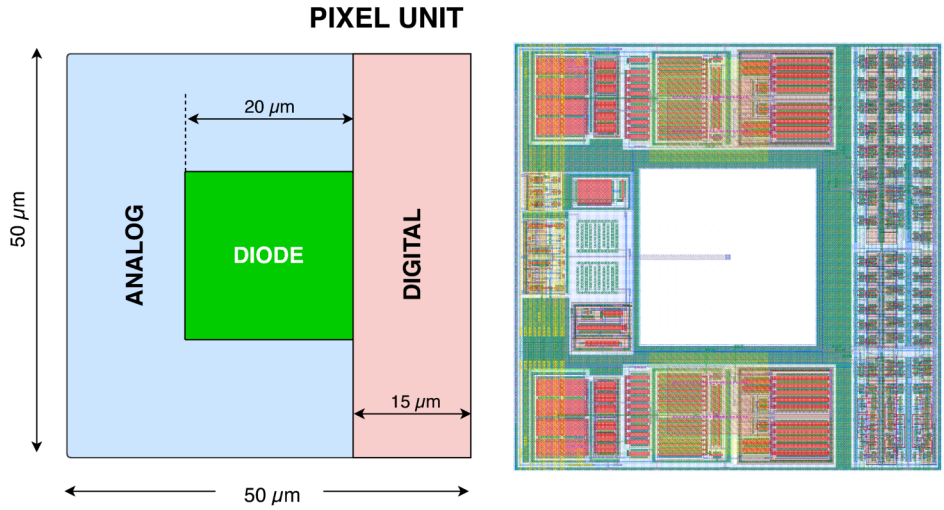


Figure 3.6: *On the left the pixel structure of MATISSE: The silicon area dedicated for the sensor is depicted in green. The area which surrounds the sensor is used to implement the analog and digital circuitry. On the right the final layout of the pixel unit.*

readout speed and the slew rate of the amplifier stage. In this version, the maximum readout speed is 5 MHz. All these requirements, together with some technical details, are summarized in Table 3.1. Since the space for the analog readout is not so large, the circuitry has been kept as much simple as possible. In the following, both the analog and the digital electronics implemented in the pixel are described.

MAIN REQUIREMENTS OF MATISSE	
Technology	CMOS BSI 0.11 μm
Voltage supply	1.2 V
Measurements	Hit position Energy Loss
Number of channels	24 $\times$ 24
Pixel size	50 μm $\times$ 50 μm
Input dynamic range	up to 24 ke$^-$
Sensor capacitance	$\sim$ 40 fF
CSA input common mode voltage	$>$ 600 mV
CSA GBW	30 MHz
CSA Slew Rate SR$^+$	20 V/μs
Local memories	2 ($\sim$70 fF each)
Noise	$<$ 100 e$^-$
Shutter type	Snapshot shutter
Readout type	Correlated Double Sampling Double Sampling
Readout speed	up to 5 MHz
Other features	Internal test pulse Mask mode Baseline regulation
Chip size	2 mm $\times$ 2 mm

Table 3.1: *Main specifications for the readout electronics implemented in MATISSE.*

3.2.1 The in-pixel analog electronics

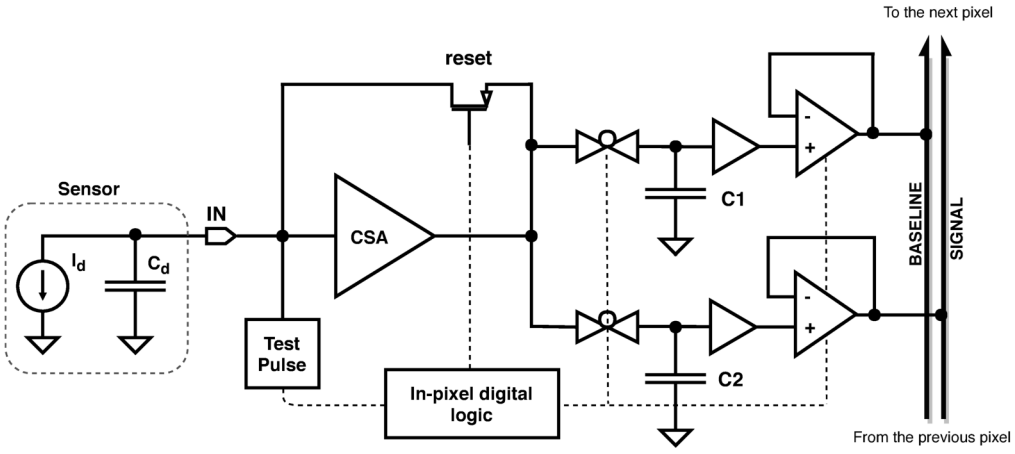


Figure 3.7: *Analog readout implemented in the pixel cell.*

The in-pixel analog readout chain, sketched in Figure 3.7, begins with the sensor where electron-hole pairs are generated by the effect of the crossing ionizing particles. After their generation, these free charges move by drift due to the electrical field applied at the bottom side. Electrons move upwards where are collected by the nwell of the channels, generating in this way the input signal of the readout chain. The signal is sent as an input to the front-end by DC coupling through a very short metal line. Generally, the signal injected to the very front-end is very weak and thus it is enhanced by means of an amplifier stage. After the amplification, the signal is sent to a sample and hold circuitry where it is stored in two MIM capacitors. The information is kept until the pixel is selected for the data transmission. This phase is managed by two analog buffers specifically developed to send data off-chip [42, 43].

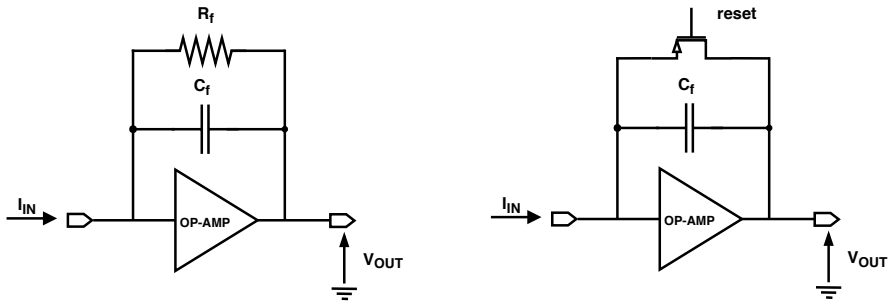
As shown in Figure 3.7, the sensor can be represented by an ideal current source with a capacitor C_d in parallel. Indeed, the collector on the top and the p^+ built at the bottom can be seen as the two capacitor arms, and in the meanwhile, the depleted volume play the role of the dielectric. A good estimation of the sensor capacitance is 40 fF. The final layout of the pixel cell is shown in Figure 3.6.

The amplifier stage

The first block of the front-end is the amplifier. Its role is to provide the interface between the events in the silicon sensor and the external world. Here the signal is am-

plified maximizing the signal to noise ratio (SNR). Different solutions can be adopted for this block such as the regulated common gate (RCG), the trans-impedance amplifier (TIA) or the charge sensitive amplifier (CSA). A Charge Sensitive Amplifier has been chosen for this purpose since it makes the readout fairly insensitive to the sensor capacitance and due to its high stability.

The response of this amplifier can be studied with the use of the ideal case depicted in Fig. 3.8a. It consists of a capacitive trans-impedance amplifier with a feedback realized by means of the capacitor C_f and the resistor R_f.



(a) **(b)**

Figure 3.8: *Simple representation of the amplification stage. On the left the TIA with a resistive and capacitive feedback and on the right the configuration used in MATISSE*

In case of ideal op-amp the open-loop gain, input impedance and bandwidth are infinite and the transfer function T(s) of 3.8a is given by:

$$T(s) = \frac{V_{out}(s)}{I_{in}(s)} = \frac{R_f}{1 + sR_fC_f} \tag{3.1}$$

If we consider the limit case where the feedback resistor R_f is infinite, or simply large as it is chosen typically in front-end amplifiers [44], the transfer function becomes the one of an ideal integrator reported in Formula 3.2. This formula shows that, under these assumptions, the feedback resistor R_f does not give any contribution to the signal processing. However, without R_f, this circuit is not DC stable and so its role in the circuit is in the stabilization.

$$\lim_{R_f \to \infty} T(s) = \frac{V_{OUT}(s)}{I_{IN}(s)} = \frac{1}{sC_f} \tag{3.2}$$

The signal generated in the silicon sensor can be approximated with a Dirac delta current pulse equal to $I_{in}(t) = Q_{in} \cdot \delta(t)$. By using Formula 3.2 and the Laplace

transform it is possible to calculate how the CSA output voltage looks like:

$$V_{out}(s) = T(s) \cdot I_{in}(s) = T(s) \cdot \mathscr{L}\{I_{in}(t)\} = \frac{1}{s\,C_f} \cdot \mathscr{L}\{Q_{in} \cdot \delta(t)\} \tag{3.3}$$

$$\mathscr{L}\{\delta(t)\} = \int_{-\infty}^{+\infty} e^{-s\cdot t} \cdot \delta(t)\, dt = 1 \tag{3.4}$$

$$V_{out}(s) = \frac{1}{s}\frac{Q_{in}}{C_f} \tag{3.5}$$

The output voltage in the time domain can be obtained taking the inverse Laplace transform of Equation 3.5 as follows:

$$V_{out}(t) = \mathscr{L}^{-1}\{V_{out}(s)\} = \frac{Q_{in}}{C_f}\,\mathscr{L}^{-1}\left\{\frac{1}{s}\right\} \tag{3.6}$$

$$V_{out} = \frac{Q_{in}}{C_f} \cdot\ \theta(t) = V_{max} \cdot\ \theta(t), \quad \theta(t) = \begin{cases} \theta(t) = 1, & t \geq 0 \\ \theta(t) = 0, & t < 0 \end{cases} \tag{3.7}$$

where θ(t) is the Heaviside step function. Equation 3.7 shows that in the ideal case the output becomes a voltage step which goes from 0 to V_{max} at t = 0 [44]. In Figure 3.9 an example of output obtained with a delta pulse injected at t_0 and t_1 is shown. V_{max} is defined by the ratio between the injected charge Q_{in} and the

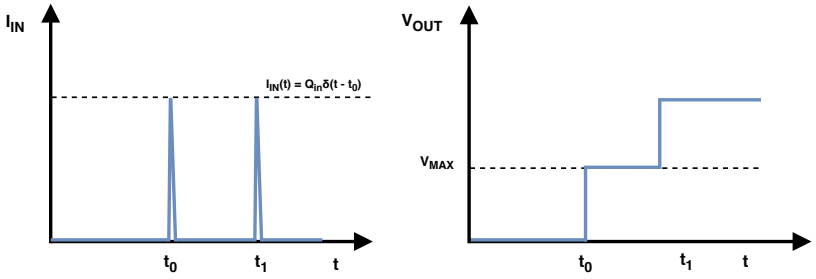


Figure 3.9: *Output voltage response of an ideal CSA to a δ-like current pulse generated at t = t_0 and at t = t_1. The output drifts upwards up to reach the saturation.*

feedback capacitor C_f. Therefore, the feedback capacitor defines the conversion gain $A_{Q_{in}\rightarrow V_{out}}$ from charge to voltage as follows:

$$A_{Q_{in}\rightarrow V_{out}} = \frac{1}{C_f} \tag{3.8}$$

The stage so far described allows to convert the collected charge to voltage but it is not yet ready to be used because after the first signal, the CSA output is never restored to the original value. This means that in case of more input signals, the pre-ampliefier goes gradually in saturation. This is what happens at t=t_1 in Figure 3.9 when the second pulse increases additionally the output voltage. The use of a switch instead of the resistor allows to solve the saturation effect. Indeed, when the switch is closed, it will discharge the feedback capacitor from the charge collected during the previous event, leaving the CSA ready for the amplification of a new signal. When it is open, the switch plays the role of a high resistance fixing the DC operation points of the circuit. The switch can be implemented with a simple transistor. This solution is extremely simple and gives a negligible increment in terms of silicon area but some attention must be paid during the design to minimize some undesirable effects introduced by the new switch such as the charge injection phenomena. Indeed, since this switch is directly connected to the input node, the possible charge injection introduced after the reset may be amplified generating undesired effects at the output. The injected charge is directly proportional to the transistor dimension, thus a PMOS transistor with the minimum size has been used to minimize this effect [45]. Figure 3.8b shows the block diagram of the CSA used in MATISSE.

The amplifier used for the CSA must meet some requirements strongly related to the silicon sensor here developed. In terms of noise, the target is below 100 e^- with a sensor capacitance of 40 fF. Another very important requirement is the common mode input voltage (CMIV) which must be kept higher than 600 mV to maximize the working region of the monolithic sensor (see Chapter 2 for more details). For what concerns the dynamic range, the CSA must be able to manage with a good linearity input signals up to 24 ke^-. In general, for the same amplifier topology, the higher is the voltage supply allowed by the technology, the higher is also the output swing. In this case, the supply voltage is 1.2 V therefore, by using a very simple solution that could be for instance an active load common source, if the overdrive voltage for both the PMOS and NMOS is 200 mV, the CSA output would have a good linearity in the range between 200 mV and 1 V. However, the open-loop gain of the common source is too small. For this reason, the configuration used to implement the core amplifier is the telescopic cascode depicted in Figure 3.10. In this description, M1 and M4 are the input transistor and the bias respectively, whereas M2 and M3 are the two cascode transistors used to increase the gain of the stage. The PMOS input transistor is sized to meet the requirement of input common mode voltage reported in Table

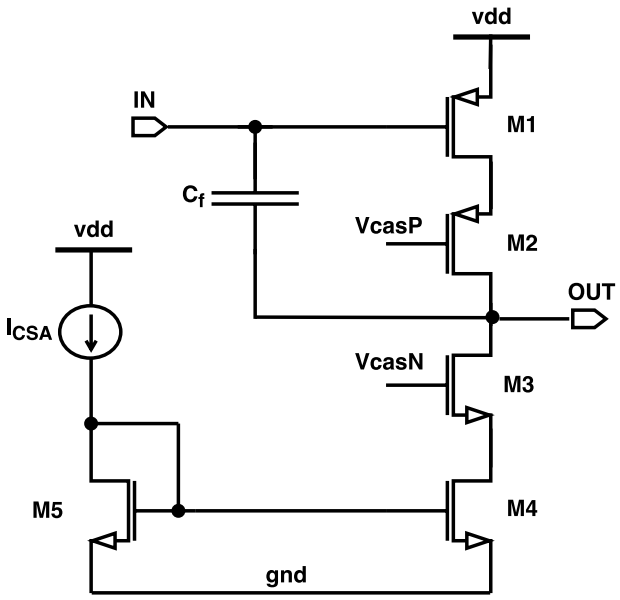


Figure 3.10: *Charge Sensitive Amplifier used in the single channel. The amplifier uses the telescopic cascode configuration.*

3.1. The open loop gain at low frequencies of the telescopic configuration is:

$$A_V = \frac{V_{OUT}}{V_{IN}} = -g_{m1}\ \frac{r_{0_{CASP}} r_{0_{CASN}}}{r_{0_{CASP}} + r_{0_{CASN}}} \tag{3.9}$$

where $r_{0_{CASP}}$ and $r_{0_{CASN}}$ are the equivalent resistances of the cascode given by:

$$r_{0_{CASP}} = r_{01} + r_{02} + (g_{m2} + g_{mb2})\ r_{01}\ r_{02} \tag{3.10}$$

$$r_{0_{CASN}} = r_{04} + r_{03} + (g_{m3} + g_{mb3})\ r_{03}\ r_{04} \tag{3.11}$$

The open loop gain of the implemented amplifier is 64 dB. Table 3.2 resumes the main parameters used to calculate this value.

The size of the input transistor and the bias have been designed taking into account important parameters like current, noise, mismatch, space and the CMIV. A design effort has been done to reduce as much as possible the contribution of noise by the input transistor so that at the CSA output it is estimated around 500 μV. The bias current is set to 1 μA to make the channel low power. Current and aspect ratio of M1 fix the voltage of the collection electrode at 820 mV. The capacitor C_f, used for the charge integration, defines the conversion gain A from charge to voltage

PARAMETER	FORMULA	VALUE	UNIT
$A_v = V_{OUT} / V_{IN}$	$-g_{m1} \cdot (r0_{CASN} // r0_{CASN})$	64	dB
$r0_{CASP}$	$r_{01} + r_{02} + (g_{m2} + g_{mb2}) \cdot r_{01} \cdot r_{02}$	100	MΩ
$r0_{CASN}$	$r_{04} + r_{03} + (g_{m3} + g_{mb3}) \cdot r_{03} \cdot r_{04}$	70	MΩ
Input resistance R_{IN}	$1/g_{m1}$	3	MΩ
Output resistance R_{OUT}	$r0_{CASP} // r0_{CASN}$	50	MΩ
Positive slew rate SR^+	-	10^6	V/s
Negative slew rate SR^-	-	0.65×10^6	V/s

Table 3.2: *Main parameters of the amplifier used in the charge sensitive amplifier.*

following the formula 3.9. For the chosen capacitance C_f=5.8 fF, the simulated gain is 150 mV/fC (schematic). However, in post layout simulations the measured value is 130 mV/fC. This difference is due to the effect of parasitic capacitances which can be compared with the small value of C_f, leading to a bigger effective feedback capacitance. This implies that for 0.6 fC (the minimum expected signal for a MIP) the expected output voltage variation is ∼78.6 mV and for 3.8 fC (the maximum expected) the expected value is ∼500 mV. These two values fix the output dynamic range of the trans-impedance amplifier. The CSA layout used in MATISSE has a rectangular shape of 19 μm × 8 μm and has been placed as close as possible to the collection electrode. Figure 3.11 shows the layout of this block.

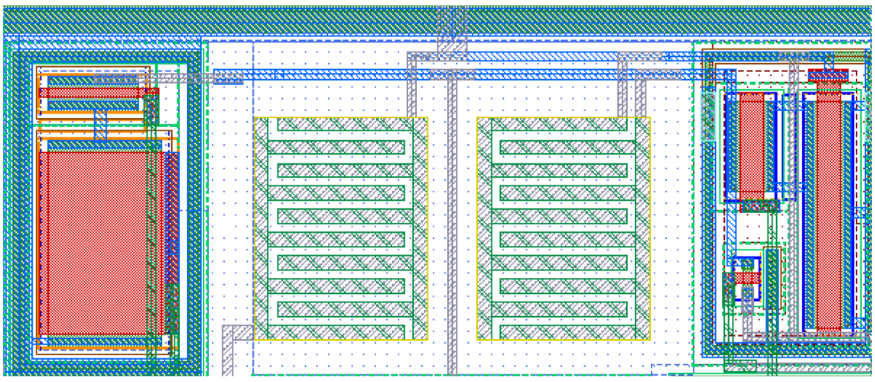


Figure 3.11: *Layout of the charge sensitive amplifier implemented in the channels of MATISSE. The block is 19 μm × 8 μm*

The sample and hold circuitry

The analog signal at the output of the charge sensitive amplifier contains the information received by the sensor and thus, it must be stored locally until the pixel is selected for the readout. This is realized by means of the sampling and hold circuit. Since the charge information is contained in the signal amplitude generated at the output of the amplifier stage, it is necessary to store two voltage values: the initial voltage after the reset which represents the baseline ($V_{baseline}$) and the voltage after the integration which may contain a signal (V_{signal}). The collected charge Q_c will be given by:

$$Q_c = \frac{V_{signal} - V_{baseline}}{C_f} \tag{3.12}$$

The voltages are stored in capacitors that as all real capacitors, are affected by a gradual loss of charge due to leakage paths generated by parasitics and due to the dielectric used in the memory which is not a perfect insulator. The effect of this leakage current is less evident in case a large charge is stored in the arm of the capacitor. Therefore, good memories are in general also big capacitances. In those applications where the pixel size is very small, most of the time only one memory can be implemented in the channel. In these cases, the baseline is captured only once at the beginning of the acquisition and is then stored off-chip or in a periphery memory for the data processing. The output (V_{signal}) is readout at the end of the integration and the baseline is retrieved from the external memory to calculate the collected charge free of reset noise [46].

The memory element used in MATISSE is implemented by means of a Metal Insulator Metal (MIM) capacitor built between metal 5 and 6. Thanks to this property, large capacitances can used even if the space is limited because the region under the capacitor can be used to built other circuitries. Two local memories of 80 fF have been placed in each pixel as shown in Figure 3.12.

The switches in the sample and hold are based on a CMOS transmission gate. This technique is used to allow a rail-to-rail operation and in the meanwhile, to reduce the effect of the charge which exists at the oxide-silicon interface of the switches when they are active. The switches are thus realized by using both PMOS and NMOS transistors driven by complementary digital signals as shown in Figure 3.13. The negative signal $\overline{sample}$ is generated at the pixel level by means of an inverter. Due to this inverter, the negative signal reaches M1 with a certain delay. To

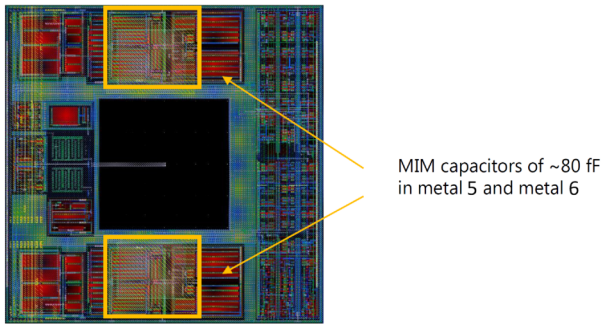


Figure 3.12: *MIM capacitors implemented in the pixel cell.*

compensate this time and to obtain the commutation of the PMOS and NMOS at the same time, the positive signal is sent to M2 by means of a delay line made by M3 and M4.

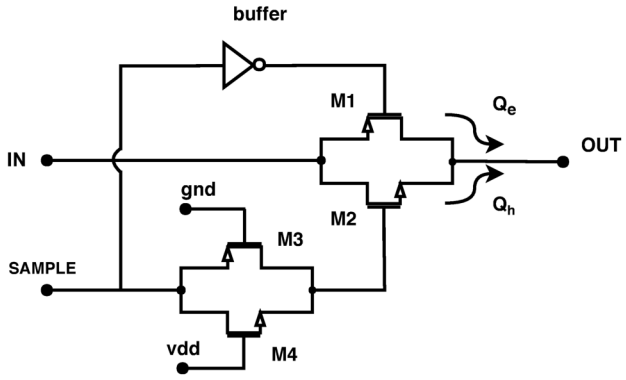


Figure 3.13: *CMOS transmission gate used in the sampling and hold implemented in the channel*

The idea behind this switch topology consist of using a second transistor with the same channel size to cancel the charge injection observed when the transmission gate turns off [47]. The charge compensation is reached when the charge injected by the NMOS (Q_e) is equal to the one which can be injected by the PMOS (Q_h). This happens when is valid the following relation:

$$W_1 L_1 C_{OX} \cdot (V_{IN} - |V_{THP}|) = W_2 L_2 C_{OX} \cdot (V_{SAMPLE} - V_{OUT} - V_{THN}) \qquad (3.13)$$

Since, Formula 3.13 is valid only for one input level, the aspect ratio of M1 and M2 have been chosen in order to compensate the charge injection for input voltages of Vdd/2 [45].

When the switches are on, their channel resistance introduces thermal noise which is added to the voltage stored in the capacitor. It can be proved that the rms noise at the output is determined by the capacitor and is approximately $\sqrt{K_B \cdot T/C_s}$. Since the sampling capacitance used in MATISSE is 80 fF, the expected noise contribution at 300 K in the stored voltage is $\sim$230 μV [44].

The analog buffers

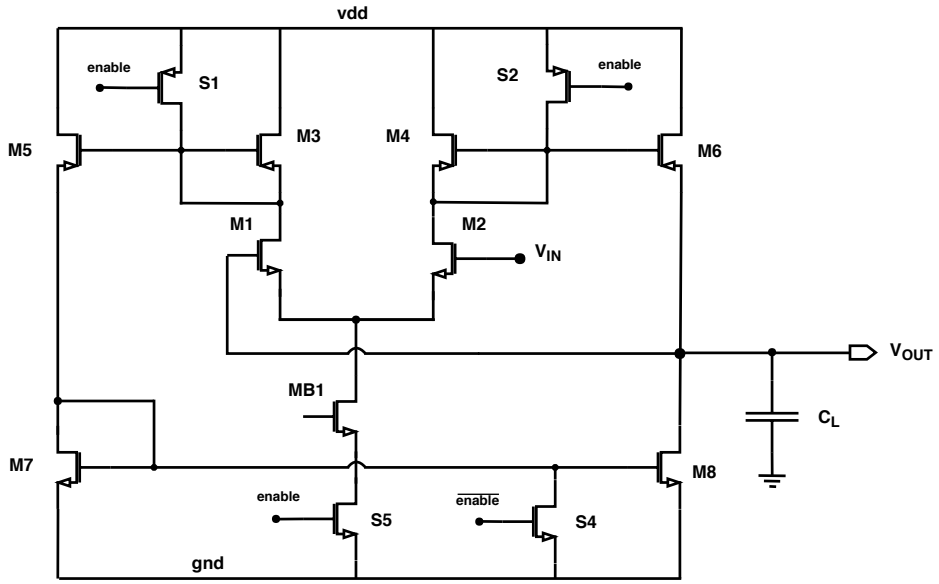


Figure 3.14: *Switched current mirror OTA used to send data off-chip*

The data stored in the sampling capacitors at a certain point, based on the readout sequence managed by the End of Column, must be sent off-chip. Therefore, a buffer is required to drive the load with negligible information loss. A common solution widely adopted to implement this block is the use of source followers [48]. These circuits exhibit a very high input impedance and low output impedance and so they could be suitable for this application. However, the input-output characteristic of the source follower is strongly dependent on the threshold voltage of the transistors and for this reason, these circuits suffer by drawbacks like non linear response and limited dynamic range. A source follower indeed shifts the dc level of the input signal by V_{GS} limiting significantly the voltage swing at the output [45]. Moreover, the technology used for the design of MATISSE allows the use of only high threshold voltage transistors which means that the minimum V_{GS} to create the channel in the

transistors is around 450 mV. This offset reduces dramatically the output swing and so the use of source followers has been considered not acceptable for this prototype. The buffer used to overcome this limitation is the switched current mirror Operational Transconductance Amplifiers (OTA) depicted in Figure 3.14.

This single stage scheme exhibits a high open loop gain and a wide input common voltage range. The OTA has been connected in negative feedback configuration in order to get the unity-gain. Transistors S1-S5 play the role of switches which enable or disable the stage based on a digital input sent by the EoC. When the buffer is off there is no current flowing through the tree branches and therefore, in the static condition, this buffer does not contribute to the power consumption of the pixel. The current gain is set by the aspect ratio of the transistors couples M3-M5 and M4-M6. The chosen gain is 5. Thanks to this current gain, most part of the current used in the buffer is transferred to the load C_L. The buffer has been designed to drive a load of 10 pF with a maximum speed of 5 MHz. To meet this requirement, the total current need by the circuit is around 300 μA. In addition to the OTA, also a low power op-amp has been used to buffer continuously the voltage stored in the memory. This block is necessary to protect the information from the spikes generated during the activation of the OTA buffer. The pixel contains in total two buffer chains, each implemented in a total area of 36 μm $\times$12 μm. As depicted in Figure 3.15, they are the largest blocks implemented in the analog in-pixel electronics.

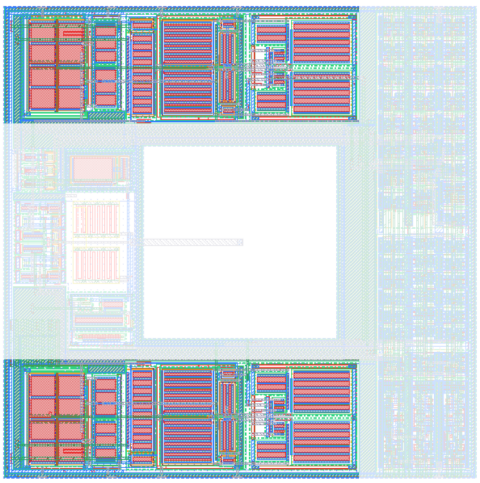


Figure 3.15: *Chain buffers used in the channel for the data transmission. Each block is 36 μm $\times$12 μm*

The baseline regulation and test pulse circuitry

The CSA has been designed to fix the polarization voltage of the collection electrode to 820 mV ($V_{in,DC}$ or CMIV). Therefore, during the reset of the capacitive feedback this voltage is transferred to the CSA output. When the reset is released, the output voltage slowly decreases until reaching the DC operating point fixed by the ohmic resistance of the reset switch. However, it may take several ms until reaching the final value making the detector initialization extremely long. For this reason, a baseline restorer is needed. On the other hand, a calibration circuit is needed in order to test the readout electronics independently by the charge collected from the sensor. For these reasons, MATISSE contains a circuitry able to restore the baseline and to generate pulses at the input of the channels. The scheme of this circuit is depicted in Figure 3.16. Both the operations are based on the injection of a certain amount of charge at the input of the CSA by means of the capacitor C_{cal}. All the operations are driven by three digital signals (S1, S2 and S3) which can be set off-chip. The amount of the injected charge is regulated by means of two reference voltages V_{TP} and V_{reg} which can be set through dedicated PADs. In case the test pulse mode is disabled by the in-pixel configuration logic, S3 is always low and thus M5 and M6 are always off. Before the regulation, M3 and M4 are off and the input of C_{cal} is connected ground by means of M1 and M2. In this condition, no charge is injected to

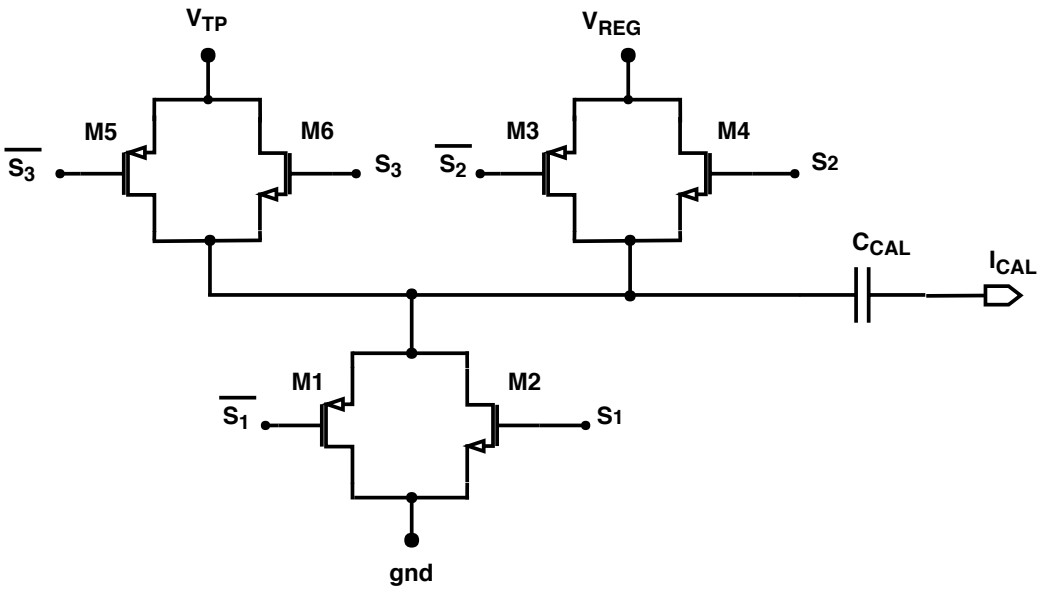


Figure 3.16: *Baseline regulation and calibration circuit*

the CSA. After the reset, the output of the pre-amplifier is high and thus, the baseline should be regulated. This operation is done by injecting charge at the input of the preamplifier. This charge injection can be realized by connecting V_{reg} at the input of C_{cal}. As a result, the output voltage of the CSA will drop by an amplitude dependent on the injected charge. If $A_{Q\rightarrow V}$ is the analog gain of the CSA, the regulated baseline $V_{baseline}$ will be:

$$V_{baseline} = V_{in,DC} - V_{reg} \cdot \frac{C_{cal}}{C_f} \tag{3.14}$$

In MATISSE both capacitances have the same value, therefore:

$$V_{baseline} = V_{in,DC} - V_{reg} \tag{3.15}$$

When the baseline is set as desired, a test pulse can be generated in the channel by means of M5 and M6. To generate a signal some charge must be extracted from the input node. This can be done by connecting the input of C_{cal} to V_{TP} which must be set lower than $V_{baseline}$. In such a way, the injected charge Q_{inj} will be negative (because extracted) and equal to:

$$Q_{inj} = (V_{TP} - V_{baseline}) \cdot C_{cal} \tag{3.16}$$

and the amplitude ΔV registered at the output will be:

$$\Delta V = (V_{TP} - V_{baseline}) \cdot \frac{C_{cal}}{C_f} = (V_{TP} - V_{baseline}) \tag{3.17}$$

Since the C_{cal} is equal to C_f, the expected voltage amplitude depends only on the two voltages which can be set from the external world. All the circuitry is managed by digital signals which are sent externally in order to guarantee the maximum versatility. The baseline can be regulated from $V_{in,DC}$ until few mV as shown in Figure 3.17. The linear response is excellent until 200 mV. Below this value, transistors M3 and M4 of the CSA go in linear region (see Figure 3.10). The maximum injected charge depends on the V_{reg} and V_{TP}. For instance, when the baseline is set to about 400 mV, the maximum injected charge is 2.44 fC which corresponds to $\sim$15000 electrons.

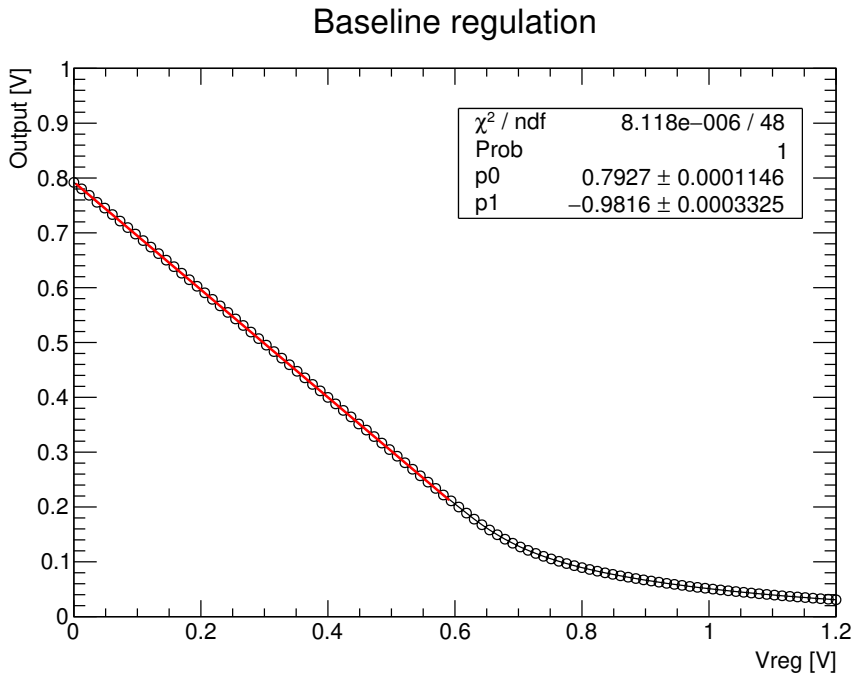


Figure 3.17: *Baseline regulation by using the V_{reg} signal.*

3.2.2 The in-pixel digital electronics

The configuration logic

Each pixel unit contains together with the front-end circuit also the necessary digital logic for the readout and the programming. This block consists of three flip-flops, some combinatory logic and several inverters used to regenerate the signals which are propagated through the columns. Flip-flops of the same topology in the same column are electrically connected to form vertical shift registers of 24 bits. The three flip-flops are the following:

- The **read flip-flop**: It is used to enable the OTA buffer in order to connect the pixel to the data transmission line. Each pixel of the columns contains one bit of this topology, all of them connected in order to form a 24 bits register. The global read reset signal (‘‘`read_reset`’’) sets the content of this register to zero. As a result, after the reset all the pixels are disconnected from the data transmission lines.

- The **TP flip-flop**: this bit is used to enable or disable the test pulse mode of the channel. When this bit goes to 1, it is possible to generate calibration pulses at the input of the front-end electronics. The pulse is injected by means of C_{cal} based on the value of V_{TP}, as explained in the previous section. By default, this option is disabled which means setting this bit to 0.

- The **$\overline{\text{MASK}}$ flip-flop**: this bit allows to switch off a pixel. This option has been introduced because very noisy pixels may disturb their neighbors degrading the performance of the whole matrix. Switching off those pixels in some cases may allow recovering the desired device performance. By default all the pixels in the matrix are on and this means setting this bit to 1.

Thanks to the last two flip-flops, MATISSE can operate in two modes:

- **Sensor Mode**: In this mode, the signals are generated into the diode and then they are processed by the electronics of the chip. This mode can be chosen writing the flip-flops of the matrix as described in Table 3.3 or simply doing the reset of the configuration bits by means of the signal ''`Prg_reset`''.

- **Test Pulse Mode**: This mode allows to generate internal pulses into those channels where the TP flip flop is set to 1. The pulses are generated at the same time in all the pixels where this mode is active. This mode can be enable by writing 1 into the TP flip-flop of the selected pixel.

In both of the readout modes described so far, it is possible to mask one or more pixels. When a pixel is masked:

- the pre-amplifier input is connected to V_{DD}, thus killing the pre-amplifier.

- the reset of the feedback capacitances by means of ''`fe_reset`'' reset signal is never issued in order to avoid unnecessary voltage swings at the pre-amplifier outputs.

- the OTA buffers are never turn on, thus reducing the power consumption.

The settings need to select the operating modes are summarized in Table 3.3.

In addition to the configuration registers, the pixel contains also a block for the local regeneration of the digital signals used inside the cell. Indeed, the digital

READOUT MODES			
FF	**Sensor Mode**	**Mask Mode**	**Test Pulse Mode**
TP	0	X	1
MASK	1	0	1

Table 3.3: *Readout modes of MATISSE*

signals coming from the EoC or from another pixel are buffered through two cascaded inverters. This allows to break the metal-lines among the columns, avoiding antenna problems where the use of more metal layers is not possible and moreover allows to send clean signals to all the pixels of the columns. Furthermore, it delays the switching from one cell to the next, reducing stresses on the power lines. Two of these additional buffers are used also to delay the flip-flop outputs in order to prevent hold time violations.

Reset signals in the pixel

Four reset signals are used in each pixel:

- Reset of the diode (‘‘`diode_reset`’’): This signal connects the pre-amplifier input to VDD, thus killing the pre-amplifier and avoiding possible oscillations when the sensor is not depleted. This option is used to protect the electronics from spikes of current which can be generated during the depletion of the diode.
- Reset of the CSA (‘‘`fe_reset`’’): It is used to reset the feedback capacitance of the front-end. This operation is routinely done at the beginning of any new integration-readout cycle to initialize the detector for a new acquisition.
- Reset of the programming registers (‘‘`Prg_reset`’’): It is used to initialize the value of the three configuration bits of the pixel. After this operation, the device is ready to work in sensor mode.
- Reset of the read registers (‘‘`read_reset`’’): It resets all the read flip flops of the matrix and the horizontal readout register placed in the EoC. As long as this reset is active, all the channels are disconnected from the transmission lines. After this reset, the readout will start always from pixel 0 and column 0.

All these reset signals are active low.

The noise injection chain

One of the goals of MATISSE is also the study of possible noise coupling between electronics and sensor which can be useful for the future design of a more complex and complete circuitry for HEP experiments or similar applications. For this purpose, a large buffer made by 18 inverters controlled by a dedicated signal is also inserted in each pixel to allow the injection of digital noise during the whole chip operation.

3.3 The end of column logic

The End of Column, called also EoC, contains the logic necessary to readout all the information contained into the pixels after an acquisition and the logic for programming the entire matrix. The block is made up of some digital cells located at the bottom of the chip in an area of 14 μm $\times$ 1225 μm physically divided from the pixel matrix by a guard-ring realized by means of a nwell connected to VDD.

For readout purposes, for each sector, the EoC contains a shift register with six cells. These cells are used to address one of the six columns of the sector during the readout. Each cell is connected to the 24 bits read register made by the flip-flops among the pixels of a column. Five of these cells are identical whereas the remaining, the cell 0, is built to allow the proper initialization of the shift register. During the readout, columns and rows are selected by means of two different clock signals which act as a pointer among the 144 pixels of each sector. The digital circuitry used for the readout procedure of a single sector is depicted in Figure 3.18.

The two clocks are the following:

- ‘‘`h_read_clk`’’: it is used to control the horizontal shift register moving the pointer from one column to the next one. This clock is delivered to all the readout cells of the EoC.
- ‘‘`v_read_clk`’’: this clock is used for the row selection during the readout. The EoC sends this clock to the selected column. Since the sectors are four, four of this clocks are propagated at the same time in the matrix allowing the parallel readout of the sectors.

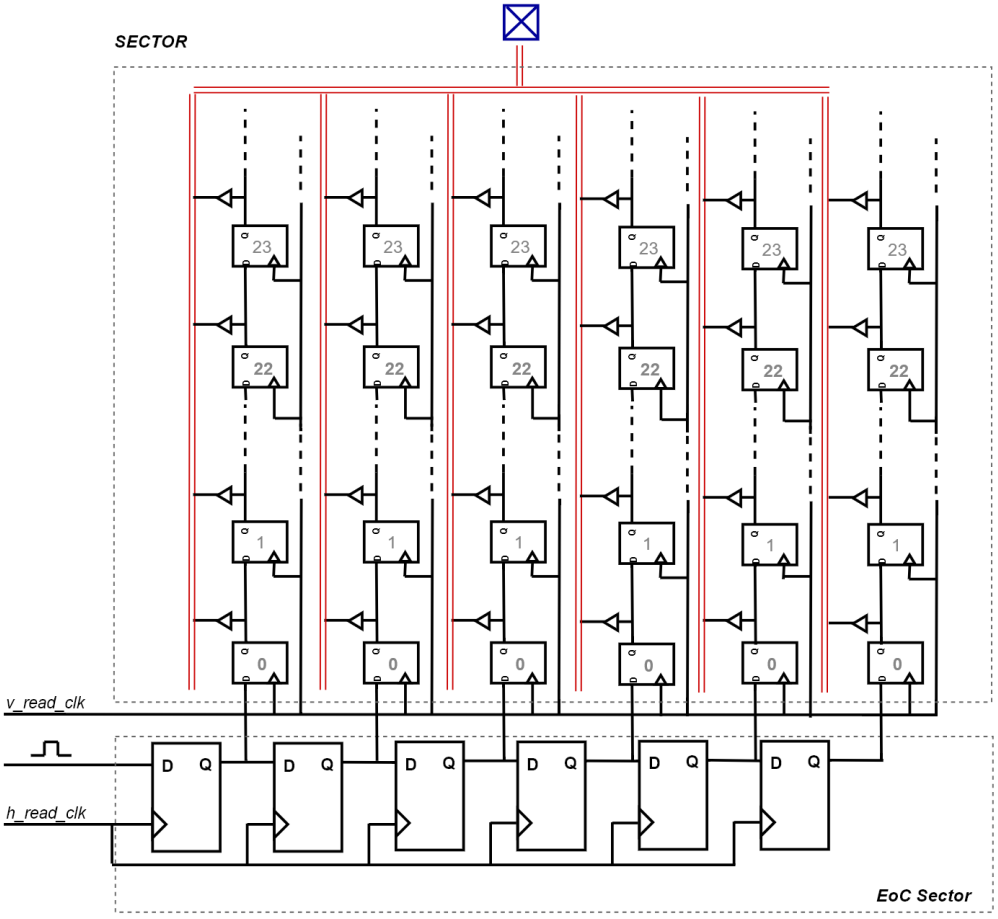


Figure 3.18: *Digital circuitry for the readout procedure of a sector*

In order to have a good control of the readout, those clocks are fed through dedicated PADs.

For what concerns the programming logic, it consists of a horizontal shift register made by 48 cells. Even cells are connected to the input of the vertical register made by the 24 MASK flip-flops, whereas odd cells are connected to the 24 bits register used to enable the test pulse mode (TP). In such a way, two contiguous cells store the programming bits (Test Pulse and Mask) to send to one column. The programming register is driven by means of the following clocks:

- "`h_prg_clk`": it is used to write the whole horizontal register according to the digital value sent to the input of the register. After 48 rising edges of this clock, the programming horizontal register is completely written. This clock is sent to all the cells of the EoC
- "`v_prg_clk`": this clock is used to shift the programming data stored in the horizontal register to the rows of the matrix. It is distributed to all the pixels of the matrix.

In order to easily control the programming phase, the input, the output and the clock of the register are accessible from dedicated PADs. Table 3.4 briefly resumes all the clock signals used in MATISSE.

DIGITAL CLOCKS				
SIGNAL	**VALUE [MHz]**			**DESCRIPTION**
	min	typ	max	
v_read_clk	1	5	7	`clock of the vertical shift register to select the pixel to be read inside a column`
h_read_clk	1	≤ 0.2	0.3	`clock of the horizontal shift register to sequentially select the column for readout`
v_prg_clk	1	≤ 20	≤ 40	`vertical clock used to program the pixel matrix`
h_prg_clk	1	500	1000	`horizontal clock used to program the pixel matrix`

Table 3.4: *Digital clocks used in MATISSE for the readout and the programming*

3.3.1 Readout operations

The readout operation of MATISSE is divided in three different steps: the initialization, the integration and the data transmission. During all the operations carried out in the first two phases, all the pixels work in parallel and there is no distinction between the sectors. On the contrary, during the data transmission, the channels does not work in parallel because they are readout through rolling shutter. The initialization phase is used to prepare the entire matrix for the acquisition of events. This is done sending a global reset of the configuration registers to initialize the matrix in the so called ''`sensor mode`'', and then sending a global reset to all the channels by means of the signal ''`fe_reset`''. After this operation, the baseline is regulated by means of the baseline regulation system. The timing for the regulation is managed by a signal called ''`baseline_reg`''. When the baseline has been regulated as desired, a global sampling is sent to the entire matrix in order to store $V_{baseline}$ in one of the two local memories. At this point starts the integration phase. The duration of the integration time is decided by means of the two sampling signals (''`SampleBsln`'' and ''`SampleSignal`'') which are accessible from the external world. The minimum integration time is in the order of few ten of nanoseconds, which is the time needed to accumulate the charge in the memories. During the integration time, if some event is recorded, the output of the amplifier changes and it can be stored in the second memory with a second sampling operation. Here ends the integration phase. At this point all the pixels of the matrix contain an information which can be seen as the snapshot of what happened during the integration phase. For this reason, these sequence of signals realize the so called snapshot shutter operation [46]. By using the readout procedure so far described the deposited charge information can be obtained by the difference between the two stored voltages. Since in these sequence the reset is performed only at the beginning, the two stored voltages are affected by correlated uncertainties generated by the reset. For this reason, their difference is not affected by the reset noise. This technique is known as Correlated Double Sampling (CDS) [46]. Since, the reset and the sampling signals can be set externally, MATISSE support also the simple Double Sampling (DS), where the reset is performed before the two sampling operations. In this case, the difference of the two voltages is affected by a noise $\sqrt{2}$ greater than the one obtained during a simple sampling [49]. Figure 3.19 shows the sequence of signals to use for the CDS or the simple DS.

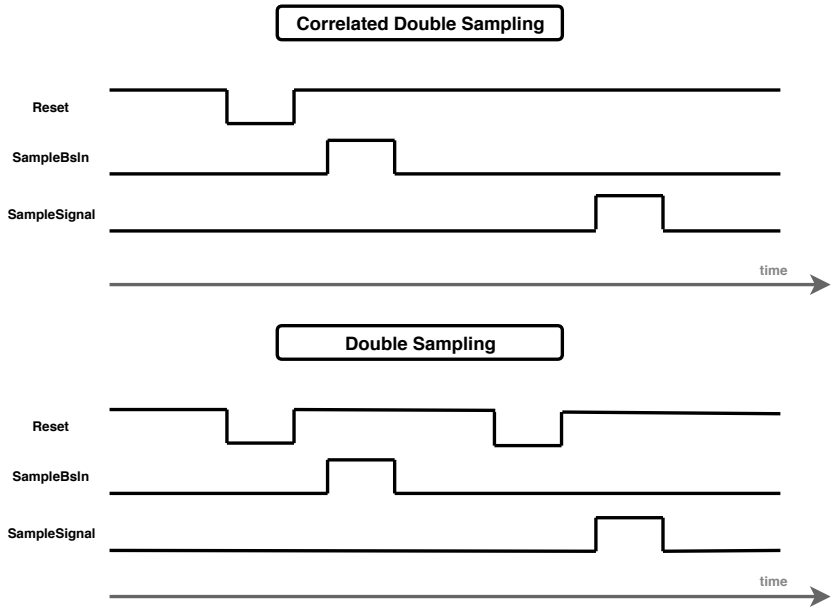


Figure 3.19: *Correlated Double Sampling (CDS) and Double Sampling (DS)*

The last step is the data transmission which is controlled by three signals: the ‘‘`read_reset`’’, ‘‘`h_read_clk`’’ and ‘‘`v_read_clk`’’. Those signals for simplicity and testability, are fed independently by means of dedicated PADs. At the beginning of the transmission the reset signal ‘‘`read_reset`’’ must be issued. When ‘‘`read_reset`’’ is low, the reset is active and the in-pixel readout flip-flops are all reset, so the readout is disabled. This is the condition during all the integration phase. When ‘‘`read_reset`’’ goes high, the reset is removed and the EoC block selects the column 0 of each sector enabling the readout cycle. The clock ‘‘`v_read_clk`’’ is propagated along the 24 in-pixel readout flip-flops of the columns and a digital pulse is injected at the input of the first one. During the first rise edge of the clock, the pixel 0 of column 0 will be connected to the two data transmission lines and the data contained in the pixel will be sent out. At each rising edge of the clock, the next pixel will be connected up to read the whole column. Thanks to the use of the digital pulse, only one pixel is connected to the data transmission lines at a given time. After a column is fully read, the ‘‘`h_read_clk`’’ will move the pointer to the next column to read in the same way its 24 pixels. This operation will be repeated until all the six columns of the sector are read. After that, the transmission cycle is completed and the ‘‘`read_reset`’’ signal can return low for the new integration phase. This logic implements the well-known rolling shutter readout.

To readout the full matrix the ‘‘h_read_clk’’ runs approximately at 1/24 the ‘‘v_read_clk’’ frequency. Since, the design of MATISSE targets to readout the columns at 5 MHz, ‘‘v_read_clk’’ is set to 5 MHz and ‘‘h_read_clk’’ to ∼200 kHz. In this condition, a single column is read in 4.8 μs and the entire matrix in 28.8 μs.

3.3.2 Programming procedure

The pixel programming is managed by an End-of-Column horizontal shift register of 48 bit and is controlled by the programming reset (‘‘Prg_reset’’), the programming clocks (‘‘h_prg_clk’’ and ‘‘v_prg_clk’’) and by the input/output of the shift register (‘‘Prg_bit_in’’ and ‘‘Prg_bit_out’’). All those signal can be set (or read) by means of PADs of the prototype.

The programming reset is used to enable/disable the programming. This reset signal is active low. If we want to program the matrix, therefore, Prg_reset must be set to 1 and kept high during all the acquisition, otherwise, all programming bits will be set to the default configuration (TP=0, MASK=1). The default values can be used if it is not needed to mask any pixel nor activate any test pulse. During the programming cycle, a pattern of 48 bits is loaded into the horizontal programming shift register by means of the configuration register input (prg_bit_in) and the horizontal clock ‘‘h_prg_clk’’. The bits are then shifted vertically towards the first pixels row (row 0) by means of the vertical clock ‘‘v_prg_clk’’, so that a new 48-bit pattern can be loaded to program the next row. These steps are repeated until the entire 24 $\times$ 24 matrix is programmed. In this way, row 0 will be programmed with the last 48-bit pattern loaded into the EoC while row 23 will be programmed with the first 48-bit pattern. In addition, while a 48-bit pattern is loaded, the previous 48-bit pattern is sent to the prg_bit_out output port, so that it is possible to read what has been written in the register. In order to properly program the entire matrix, the frequency of ‘‘v_prg_clk’’ must be equal to ‘‘v_prg_clk’’/48.

With a frequency of ‘‘h_prg_clk’’ equal to 50 MHz and the one of ‘‘v_prg_clk’’ equal to 10 MHz the pattern of 48 bits is loaded into the horizontal shift register in 96 ns and the full matrix is programmed in 2.3 μs.

3.3.3 Pad frame and pinout

The pinout of MATISSE is shown in Figure 3.21. It is composed by 59 pads used for the following purposes:

- 7 pads used for the bias: 3 currents and 4 voltages
- 8 pads dedicated to the analog outputs. All of them are located on the top side
- 1 pad for a single digital output
- 14 digital control pads: they form a group located on the bottom side
- 29 pads used for the voltage supplies and grounds

The chip has 8 analog outputs and as explained previously they are used to estimate the charge collected into the pixel diodes. Since this information is really important for the diode characterization, from a design point of view some efforts have been done to avoid influences from noisy sources such as the digital logic. For this reason in the pinout all the digital pads (inputs and outputs) forms a single block divided from the analog domain by three breakers: 2 on the lower left and 1 on the lower right. Some efforts have been done also in the analog domain where the most important part of the front-end, the pre-amplifier, has been divided electrically from the rest of the electronics. The breakers on the upper left and upper right are used to allow this additional separation. Due to the five breakers the pinout appears divided in four blocks. For each block, all the protection diodes should be polarized properly and this can be done by setting the voltage of all the pads indicated with the type VSS IO, VDD IO, VSS CORE and VDD CORE in Table 3.5 and 3.6. The following pictures and tables describe all the pads of MATISSE.

TOP SIDE				
N	**PIN NAME**	**PAD TYPE**	**PURPOSE**	**DESCRIPTION**
1	gnd_1	**VSS CORE**	GROUND	Ground.
2	outBsln_1	ANA I/O	ANALOG OUTPUT	Output for the baseline for the sector 1.
3	gnd_2	**VSS CORE**	GROUND	Ground.
4	outSignal_1	ANA I/O	ANALOG OUTPUT	Output for the signal for the sector 1.
5	gnd_3	**VSS CORE**	GROUND	Ground.
6	outBsln_2	ANA I/O	ANALOG OUTPUT	Output for the baseline for the sector 2.
7	gnd_4	**VSS CORE**	GROUND	Ground.
8	outSignal_2	ANA I/O	ANALOG OUTPUT	Output for the signal for the sector 2.
9	gnd_5	**VSS CORE**	GROUND	Ground.
10	outBsln_3	ANA I/O	ANALOG OUTPUT	Output for the baseline for the sector 3.
11	gnd_6	**VSS CORE**	GROUND	Ground.
12	outSignal_3	ANA I/O	ANALOG OUTPUT	Output for the signal for the sector 3.
13	gnd_7	**VSS CORE**	GROUND	Ground.
14	outBsln_4	ANA I/O	ANALOG OUTPUT	Output for the baseline for the sector 4.
15	gnd_8	**VSS CORE**	GROUND	Ground.
16	outSignal_4	ANA I/O	ANALOG OUTPUT	Output for the signal for the sector 4.

RIGHT SIDE				
N	**PIN NAME**	**PAD TYPE**	**PURPOSE**	**DESCRIPTION**
17	VBsln_regulator	ANA I/O	ANALOG INPUT	Voltage to set the baseline.
18	VTP	ANA I/O	ANALOG INPUT	This sets the amplitude of the test pulse.
19	pCas	ANA I/O	ANALOG INPUT	Bias for cascode p-type.
20	nCas	ANA I/O	ANALOG INPUT	Bias for cascode n-type.
21	vdd_buff_1_b	**VDD I/O**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 1.
-	BREAKER	BREAKER	BREAKER	Breaker.
22	vdd_buff_2_b	**VDD CORE**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 2.
23	gnd_9	**VSS I/O**	GROUND	Ground.
24	vdd_preamp_b	**VDD I/O**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the preamplifier.
25	gnd_10	**VSS CORE**	GROUND	Ground.
26	vdd_grdr_b	ANA I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the guardring.
27	gnd_11	**VSS CORE**	GROUND	Ground.
-	BREAKER	BREAKER	BREAKER	Breaker.
28	prg_bit_out	ANA I/O	DIGITAL OUTPUT	Programming bit output.
29	vdd_dig	**VDD I/O**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for digital logic parts.
30	gnd_eoc	**VSS I/O**	GROUND	Ground.

Table 3.5: *Pinout of MATISSE: top side and right side.*

BOTTOM SIDE				
N	**PIN NAME**	**PAD TYPE**	**PURPOSE**	**DESCRIPTION**
31	gnd_eoc_2	**VSS I/O**	GROUND	Ground.
32	TP	ANA I/O	DIG INPUT	Test pulse for the input signal.
33	Bsln_regulator_ctrl	ANA I/O	DIG INPUT	Control signal for the baseline.
34	SampleSignal	ANA I/O	DIG INPUT	Sampling signals for the input signal.
35	SampleBsln	ANA I/O	DIG INPUT	Sampling signals for the baseline.
36	ResetRead	ANA I/O	DIG INPUT	Bit to force to zero all the read flip flops (active low).
37	ResetPrg	ANA I/O	DIG INPUT	Bit to force the TP and mask register (active low).
38	feReset	ANA I/O	DIG INPUT	Front-end reset (active low).
39	DiodeReset	ANA I/O	DIG INPUT	Initialization chip bit (connect the diode to vdd).
40	Digital_in	ANA I/O	DIG INPUT	DIG INPUT for the digital noise stage; if not used, connect it to the ground.
41	v_read_clk	ANA I/O	DIG INPUT	Vertical readout clock signal.
42	h_read_clk	ANA I/O	DIG INPUT	Horizontal readout clock signal.
43	v_prg_clk	ANA I/O	DIG INPUT	Vertical programming clock signal.
44	h_prg_clk	ANA I/O	DIG INPUT	Horizontal programming clock signal.
45	prg_bit_*in*	ANA I/O	DIG INPUT	DIG INPUT programming bit.
46	vdd_dig_2	**VDD I/O**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the digital logic parts.

LEFT SIDE				
N	**PIN NAME**	**PAD TYPE**	**PURPOSE**	**DESCRIPTION**
47	gnd_eoc_3	**VSS I/O**	GROUND	Ground.
48	vdd_dig_3	**VDD I/O**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the digital logic parts.
-	BREAKER	BREAKER	BREAKER	Breaker.
-	BREAKER	BREAKER	BREAKER	Breaker.
49	gnd_12	**VSS CORE**	GROUND	Ground.
50	vdd_grdr	ANA I/O	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the inner guardring (NWELL).
51	gnd_13	**VSS CORE**	GROUND	Ground.
52	vdd_preamp	**VDD I/O**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the preamplifier.
53	gnd_14	**VSS I/O**	GROUND	Ground.
54	vdd_buff_2	**VDD CORE**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 2.
-	BREAKER	BREAKER	BREAKER	Breaker.
55	vdd_buff_1	**VDD I/O**	VOLTAGE SUPPLY (1.2 V)	Voltage supply for the buffer 1.
56	gnd_grdr	**VSS I/O**	GROUND	Ground.
57	biasPreamp	ANA I/O	ANALOG INPUT	Bias for the preamplifier.
58	biasBuffer2	ANA I/O	ANALOG INPUT	Bias for the buffer 2.
59	biasBuffer1	ANA I/O	ANALOG INPUT	Bias for the buffer 1.

Table 3.6: *Pinout of MATISSE: bottom side and left side.*

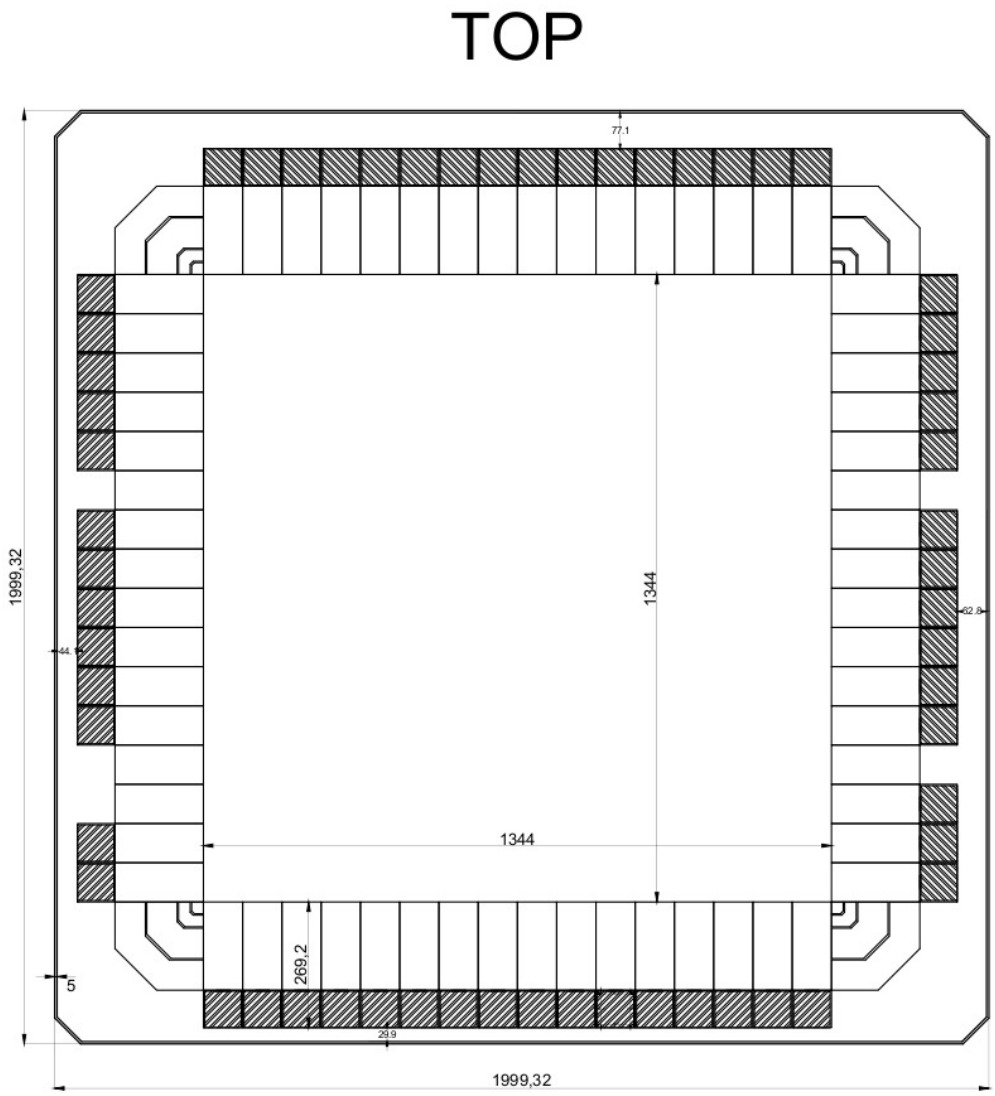


Figure 3.20: *Dimensioning of MATISSE.*

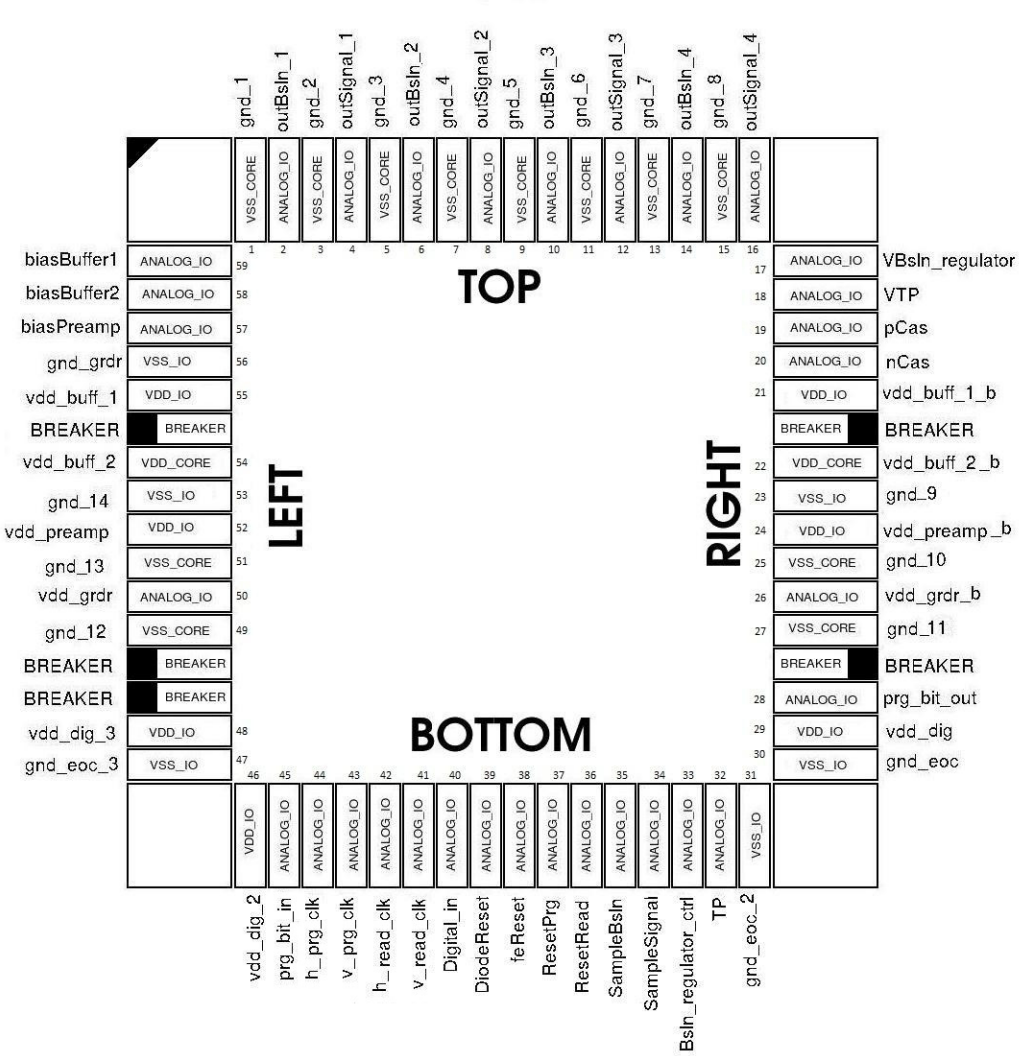


Figure 3.21: *The pinout of MATISSE.*

Chapter 4

Experimental results

The first prototypes of MATISSE and test structures have been submitted to the foundry for fabrication on April 2016. Two fabrications steps have been required to get the complete sensors which have been received on April 2017.

The first part of this chapter is dedicated to the description item by item of the DAQ system and the boards specifically developed by the INFN of Padova for the characterization phase. After this introduction follows the description of the main measurements done for the characterization of the test chip. Here are discussed the properties of the sensors from three different wafers labelled wafer 18, 19 and 24. The depletion voltage has been analyzed together with the leakage current by using the results from the test diodes, matrices and MOS capacitors. Particular attention has been put on the characterization of the latter because it allowed extracting useful information about the backside layers which explained unexpected results. A dedicated irradiation test has been done to prove some theories obtaining good results. In the second part of this chapter, the results from the characterization of MATISSE are discussed. First, the sensor performance is examined by means of I-V and C-V curves and then, the results of the readout electronics characterization are described. Important quantities like noise, linearity, dynamic range and power consumption have been measured by means of internal pulses generated at the pixel level. At the end, the complete monolithic device has been tested in condition of full depletion by using external sources like X-rays, lasers and active sources. The results coming from this tests are reported and discussed.

4.1 The Data Acquisition System (DAQ)

The data acquisition system consists of all the hardware and software used for the characterization of a prototype. Usually each chip, based on the data format which sends to the external world, has a dedicated DAQ controlled by software developed in programming languages like LabView, C++, C, Fortran and so forth. Even though the MATISSE prototypes and the test structures are based on the same silicon sensors, they need a completely different DAQ systems for their characterization. The simplest one is used for the test structures. In this case indeed, the interesting information are currents, voltages and capacitances which can be directly measured by means of the diodes and capacitors built on the test chip. For this reason, the hardware consists of a basic PCB without any electronics on board (an example is shown in Figure 4.1) and all the required instrumentation to measure with high precision the fundamental quantities. Currents and voltages are measured by means of a High Voltage Source-Measure Unit (Keithley 237) able to reach voltages up to 1000 V. The capacitance is measured with an high precision RLC meter (HP4284A). All the instrumentation is controlled by a software wrote in LabView.

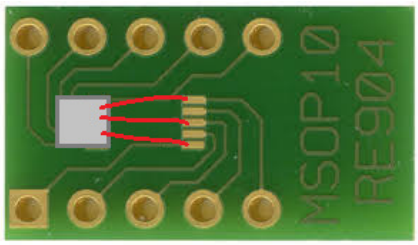


Figure 4.1: *Example of test board used for the characterization of the test structures. The samples are glued to the board to contact the top or the bottom based on the parameter which is under study. In some cases wire-bonding has been used to interconnect prototype and test board.*

The DAQ used for the prototypes of MATISSE is more complex. The whole system in this case is based on a modular approach which made possible to divide in independent steps the ASIC and the DAQ design. The DAQ system is composed by three main parts here described separately: a printed circuit board (PCB), a versatile DAQ-box and a software based on ROOT [50] and C++. Figure 4.2 shows the schematic representation of the whole system.

The PCB design aimed to built a versatile board capable to be reused to test rapidly several samples. For this reason the PCB consist of a small board, called

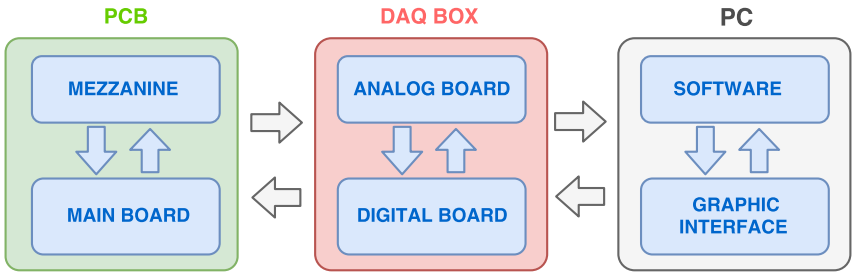


Figure 4.2: *Main blocks of the DAQ system used for the characterization of MATISSE.*

mezzanine, and a motherboard (MB). The mezzanine acts as mechanical support for the chip. Here each sample is first glued and then connected to the PCB PADs through the wire-bonding technique. Mezzanines are small and therefore also easy to handle during the chip assembly. In fact they contain only the essential discrete devices needed by the chip for the communication with the motherboard. Thanks to these properties a large number of mezzanines have been quickly prepared for the characterization.

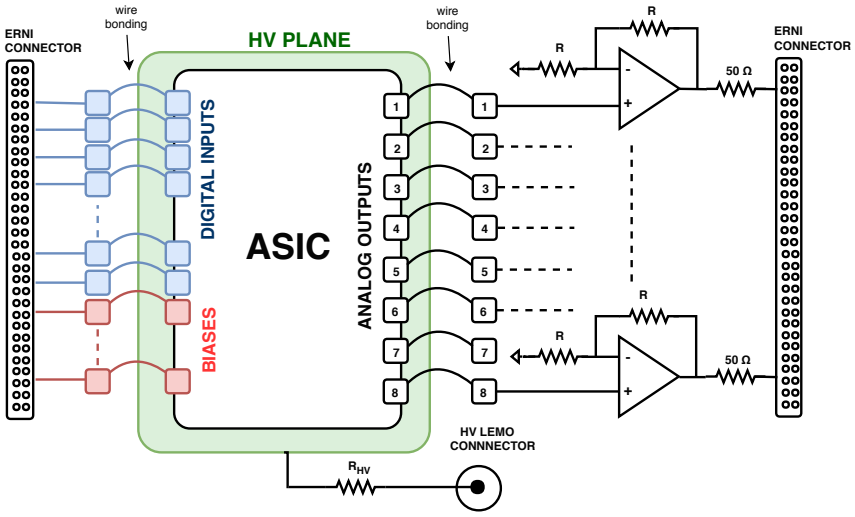


Figure 4.3: *Electronics mounted on the mezzanine.*

Eight analog buffers are mounted on the mezzanine (Figure 4.3) which take the analog information generated by the prototype and send it to the motherboard. Each buffer is implemented with a differential amplifier (AD8012AR) connected in non-inverting configuration. At this level of the chain the signal is amplified by a factor 2 in order to make the hardware compatible with fifty-ohm systems. In addition to the buffers, the mezzanine contains also a simple circuitry to provide the high voltage.

As shown in Figure 4.3 this circuitry is composed by a LEMO connector and a 1 kΩ SMD resistor which sets the maximum current flowing in the HV domain. On the mezzanine are also placed two 50 pin ERNI-SMC connectors of 1.27 mm pitch used for the interconnection with the motherboard. The one depicted on the left side of Figure 4.3 is used for the digital communication between the chip under test and the motherboard, to lead the supply voltages and all the voltages/currents needed to bias the chip. For what concerns the connector depicted on the right side, it is used to send the buffered analog signals to the carrier board.

The main board contains all the discrete devices needed for the complete characterization of the detector and therefore is much bigger than the mezzanines. All the electronics here contained can be divided into three categories:

- **The supply voltage generation circuitry:** The 1.2 V voltage needed to supply the detector is generated at this level through two low-dropout voltage regulators (LDO). Since one of the goals of the characterization is the study of the effects generated by a fast digital logic in the analog pixel circuitry, analog and digital power domains are generated independently. Figure 4.4 shows the schematic diagram used for the power generation of both domains. Note that in order to generate 1.2 V, the intermediate 3.3 V has been generated because is required by some discrete devices on the motherboard.

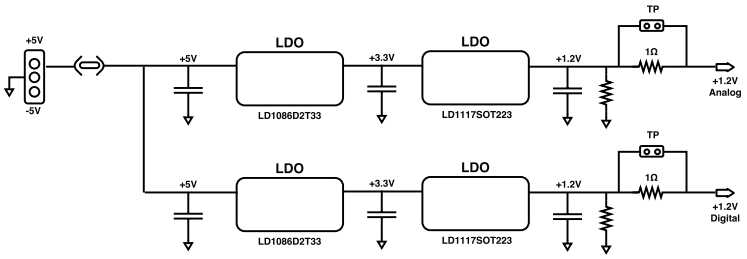


Figure 4.4: *Analog and digital power domain generation on the carrier board.*

- **The bias generation circuitry:** MATISSE needs three currents and four voltages which are generated by the main board. Those biases can be regulated through trimmers or by means of a 12 bit DAC with 16 channels (AD5391BSTZ-3) programmed with the I^2C communication protocol. A jumper on the motherboard is used to select the regulation mode for each bias. Before being sent to the mezzanine, the bias voltages are buffered by differential amplifiers (OP4177ARZ).

- **Manual reset:** Two buttons are placed on the board to manually reset all the front-ends and all the registers of the matrix. This option has been added to simplify the debug operation in case of problems during the characterization.

- **The digital signals conversion circuitry:** Digital inputs are generally carried differential or semi-differential specially in high-speed circuits where low power and low noise data transmission are required [51]. For this reason the main-board has been designed for LVDS (Low Voltage Differential Signaling) digital inputs. However, the prototypes have been produced in CMOS 1.2 V technology and therefore, it is necessary to convert the LVDS digital input into the CMOS 1.2 V format needed to control the readout operations of the detector.

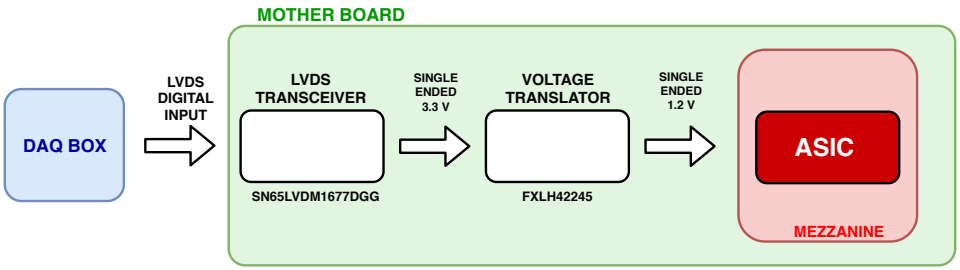


Figure 4.5: *Digital inputs conversion chain.*

Figure 4.5 shows the conversion chain used to generate the digital inputs of MATISSE. The digital input is received through a 50-pin ERNI-SMC connector in LVDS format and is sent to a transceiver (SN65LVDM1677DGG) which generates a 3.3 V single ended signal. This new signal is sent to a level shifter (FXLH42245) which attenuates the signal amplitude to 1.2 V as required by the CMOS technology. In the same way the digital output generated by the prototype is converted first in a 3.3 V CMOS signal and then to the differential LVDS format.

- **The circuitry for the analog data transmission:** The main board receives the analog signal from the mezzanine and send it to the DAQ system in two different ways: in single-ended format or differential. In the first case eight single-ended signals (two for each sector of the matrix) are sent out by means of LEMO connectors placed on the motherboard. This option has been though to connect the motherboard directly with an oscilloscope but is not the optimal solution if one needs to send information for long distances. In that case,

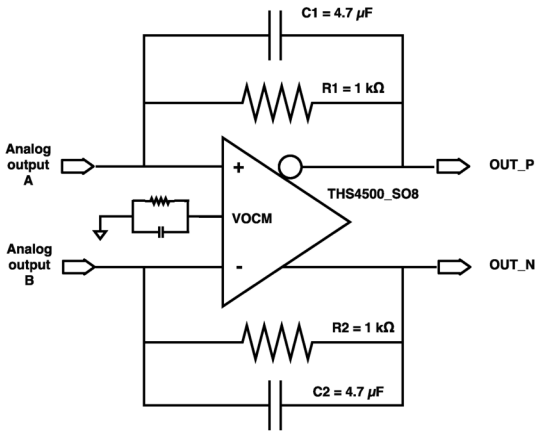


Figure 4.6: *Schematic of the differential amplifier used to send the information to the DAQ box*

the differential format is preferred because is more robust against external interferences. Differential signals are generated on the main board by means of the analog outputs of each sector and are sent to the DAQ through USB connectors. The circuitry used to generate the differential signal is shown in Figure 4.6.

Figure 4.7 shows both the mezzanine and the motherboard so far described.

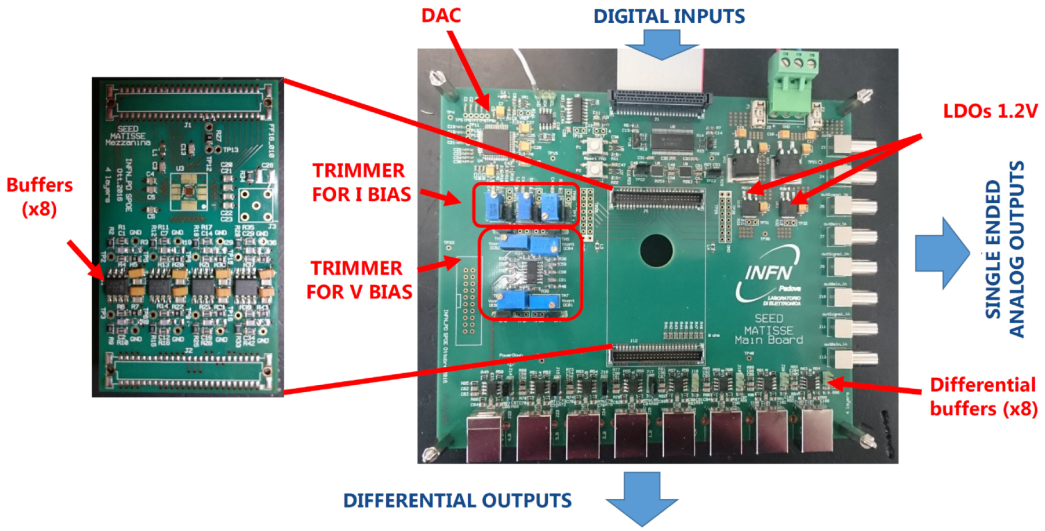


Figure 4.7: *Top view of the mezzanine (on the left) and motherboard (on the right).*

The DAQ-box [52] used for the characterization has been developed by the INFN section of Padova to cope with the need of having a versatile system able to drive and

read different detector designs. The system is small and compact since all the cabling has been optimized as much as possible. This block generates the digital stimuli used to control the ASIC and reads its analog response by using respectively a digital and an analog board. The digital card is composed by a commercial FPGA, a local clock generator, a 64 bit access bus DDRAM and a set of communication solutions like USB, Rocket IO and Ethernet. The FPGA currently mounted is the Xilinx Virtex 5 but thanks to the modular approach used to built this whole system it can be replaced by the latest version without redesign the digital board. The communication with the control PC is done through a USB cable with a maximum communication speed of 25 Mbyte/s depending on the USB controller mounted on the computer. The I/O communication with the motherboard is implemented by dedicated LVDS lines (16 inputs and 16 outputs) with a maximum speed of 630 Mbps. This connection has been done with commercial USB cables.

The analog board contains 5 independent channels each with a 100 MS/s 14 bit Analog to Digital Converter (ADC). The ADCs are clocked to a fixed 100 MHz clock generated in the digital board and also available as digital output. This part of the DAQ system is the most critical in terms of noise therefore an effort has been done during its designed in order to minimize the noise contribution as much as possible. Analog and digital boards are connected through two SAMTEC connectors and are placed together with all the necessary power supplies into the rack-module box shown in figure 4.8. For more details see [52].

Figure 4.8: *Picture of the DAQ box used for the characterization.*

The firmware used for programming the FPGA manages the communication between all the blocks of the system and controls the acquisition phase: the data coming from the ADCs are first serialized and then stored into a local 64k words FIFO. The stored information are packed according to the sensor geometry saving also additional information like position in the matrix array and pixel counts. Data is then sent to the PC through a USB connection.

The software installed on the computer takes the information contained in the data packets sent by the DAQ-box and returns the physical layout of the pixel array. In such a way the matrix map can be reconstructed in real time. The software is completely based on ROOT GUI classes and C++ and therefore it can be easily controlled by the user. Online acquisition is possible and some data analysis can be done online by using all the benefits of the ROOT environment. A snapshot of the GUI is shown in Figure 4.9

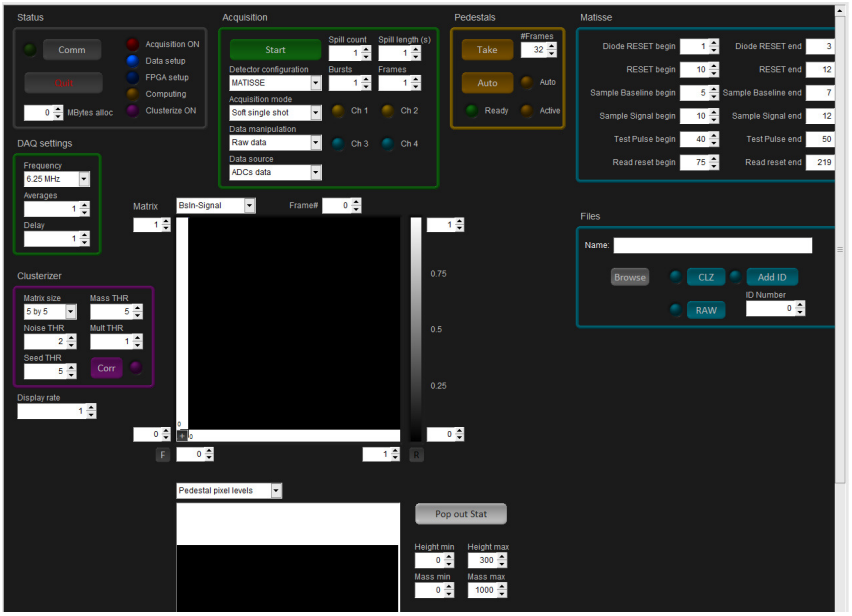


Figure 4.9: *Graphical interface of the software used for the characterization.*

4.2 Characterization of test structures

The prototype with test structures has been developed to study in detail some properties both of the sensor and the technology. Three different structures have been implemented: diodes, empty matrices and a MOS capacitor. Diodes and matrices are built mostly in the same way: they have a metal terminal and a guard-ring on the backside and the collector terminal on the top. All diodes share the same collector node made by an array of PADs built the top. For the diodes characterization, the samples have been placed on a test board bottom up by using a conductive epoxy glue to connect the array of PADs with the metal plane of the test board. In such way all the backside is accessible from the top and the nwell can be biased by a connector placed on the PCB. The collector terminal of the matrices is different: in this case pixels belonging to the same matrix have this terminal shorted and connected to a the same PAD. The matrices are three and so in total there are three PADs for the collector nodes which can be reached by means of wire-bonding. Since the chip topside must be reachable from the top, the backside has been glued to the test board. The chip assembly for the characterization of the MOS capacitor is similar to the one used for the test diodes. The gate terminal, where the polarization voltage must be applied, is on the backside and thus in this case, the sample has been connected to the test board bottom up. The nwell terminal is used to set the bias of the bulk. Figure 4.10 briefly resumes the chip assembly used in the three cases.

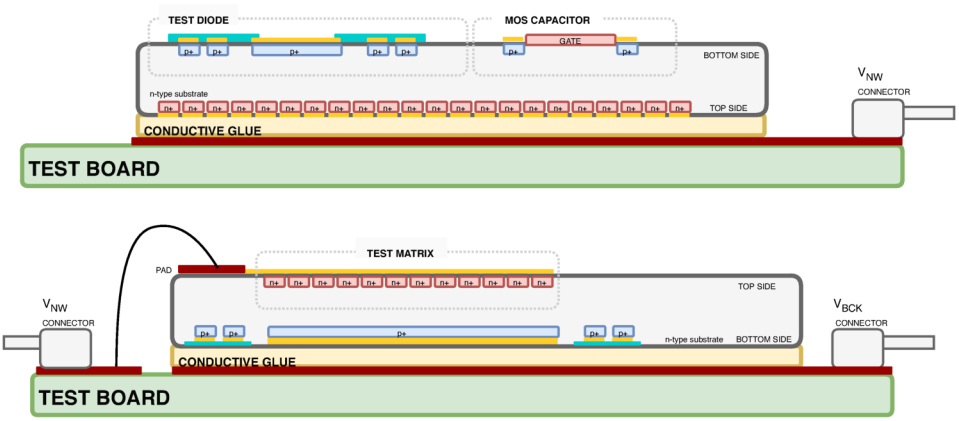


Figure 4.10: *Chip assembly configurations used for the characterization of the test structures. At the top is shown the configuration used to test diodes and the MOS capacitor. At the bottom the configuration used to test the matrices.*

4.2.1 Quality inspections of the backside layers

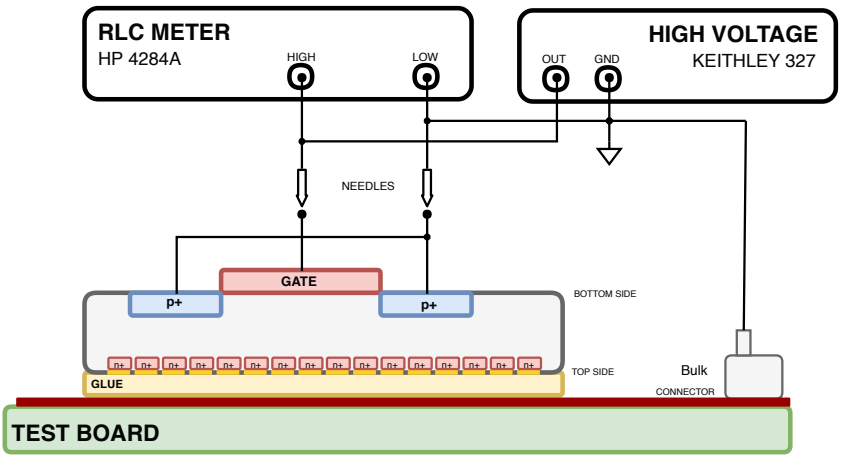


Figure 4.11: *Scheme used to measure the capacitance of the MOS*

The sensors developed in the SEED project are based on the double side processing since the two fabrication phases are fundamental to obtain fully depleted sensors. In particular, the fabrication of the backside is very important because here are built the guard-rings which determine fundamental sensor parameters like depletion and breakdown voltage. The properties of the guard-rings may depends a lot on the quality interface between the silicon substrate and the thin insulator built on the backside. A test structure has been built on this side for determining its quality. The selected structure is a MOS capacitor built with the same insulator used to produce all the structures of the backside. Measurements on the MOS capacitor can give very useful information about the properties of the insulator. In this context the capacitance-voltage (C-V) measurement is a powerful tool commonly used to determine the gate oxide thickness, substrate concentration, flat-band and threshold voltage.

For the MOS characterization, a sample from wafer 18 (MOS18) and wafer 19 (MOS19) have been used. The samples have been glued bottom up on an empty test board and the gate terminals have been biased by means of a probe station needle. The conductive epoxy glue used for the chip assembly allows to easily contact the n^+ terminal by means of a connector placed on the board. During the measurement, two different sweep voltages have been applied to the p+ terminal: a positive sweep from -20 V to +20 V and a negative from +20 V to -20 V. The n^+ contact has been simply

connected to ground. The capacitance has been measured through a high precision RLC meter (HP4284A) by following the measurement setup depicted in Figure 4.11.

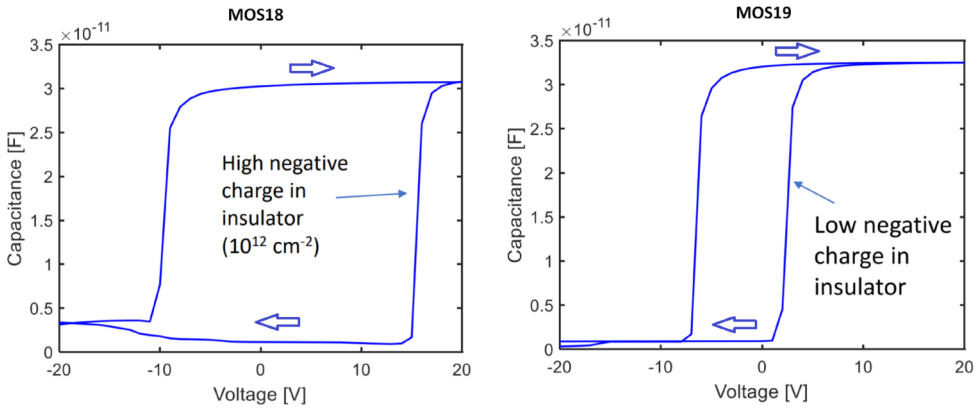


Figure 4.12: *C-V characteristic of the MOS capacitor built on wafer 18 (left) and wafer 19 (right). An hysteresis is clearly observed most probably due to unexpected charge in the oxide layer. Arrows indicate the sweep direction used during the measurement.*

The C-V curves obtained from the two samples are reported in Figure 4.12. The first thing to notice by looking at the curves is a clear hysteresis which seem to be more evident in MOS18. Ideally positive and negative sweeps should give the same result but here the sweep direction plays a important role. The measured threshold voltage V_{TH} in fact depends on the sweep direction used for the measurement. In MOS18 the threshold is -10 V and +15 V for positive and negative sweeps respectively, whereas in MOS19 the values are -7 V and +2 V. Since same results have been obtained with other samples from the same wafers, it is assumed that there is an important difference between the wafers themselves. It is known that there is a small difference of $\sim$10 μm, between their thickness and this leads to different values of C_{MAX} as observed in Figure 4.12. However, the thickness difference does not explain neither the hysteresis itself nor the different results of the wafers.

The hysteresis is attributed to trapped charge in the thin insulator layer during the voltage sweep. To explain this effect let's study what happens in the MOS capacitor during the sweep operation.

Figure 4.13 shows the fundamental working regions of the MOS capacitor for different gate voltages: accumulation, depletion and inversion. These regions are determined by means of two important parameters called threshold voltage V_{TH} and flat-band voltage V_{FB}. In devices built on n-type substrates, the threshold voltage

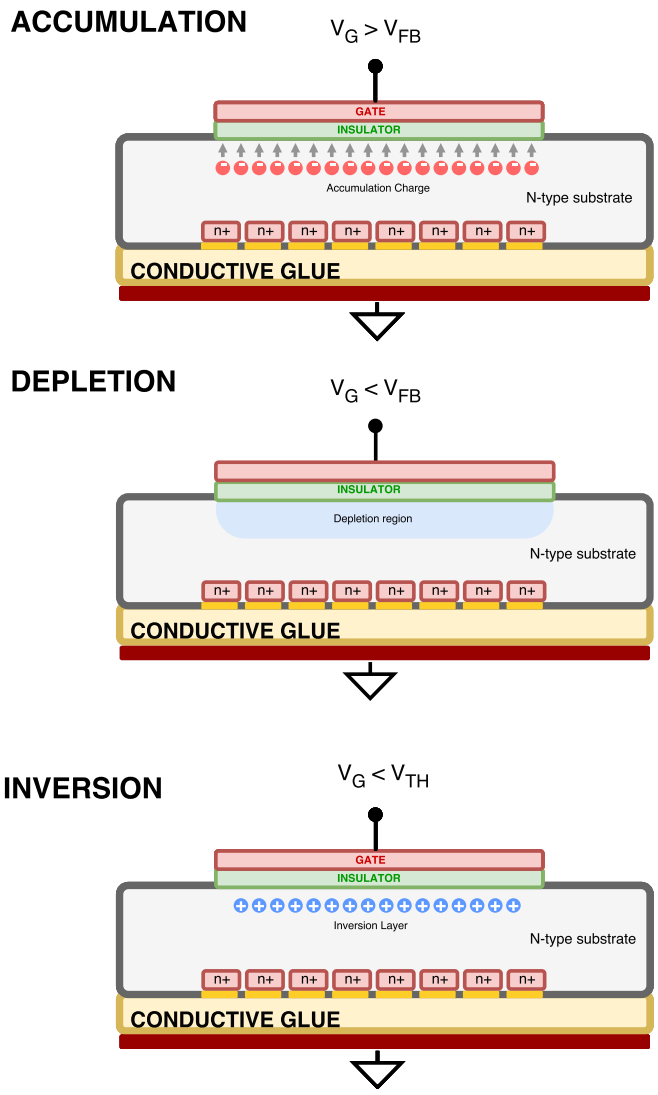


Figure 4.13: *MOS capacitor in accumulation, depletion and inversion.*

is defined as the voltage to apply to the gate in order to make the surface hole concentration n_s equal to the bulk doping concentration N_D. The second parameter, the flat-band voltage, is defined as the gate voltage which makes flat the energy bands (Ec and Ev) of the substrate at the insulator interface [53].

When the voltage $V_G > V_{FB}$ is applied to the gate, the surface electron concentration below the insulator increases and becomes higher than the bulk electron concentration. In this condition the MOS works in accumulation of negative charge (Q_{ACC}) and the capacitance of the device becomes:

$$C_{OX} = -\frac{Q_{ACC}}{(V_G - V_{FB})} \tag{4.1}$$

Thanks to the material properties used to built the device, normally the accumulated charge can not pass through the insulator. For instance in the case of having a structure made by poly/SiO_2/P-substrate, the electron affinity of the material leads to have an energy barrier in the Si/SiO_2 interface of 3.1 eV and 4.8 eV for electrons and holes respectively. Figure 4.14 shows the energy bands of this structure when the gate voltage matches the band-flat voltage.

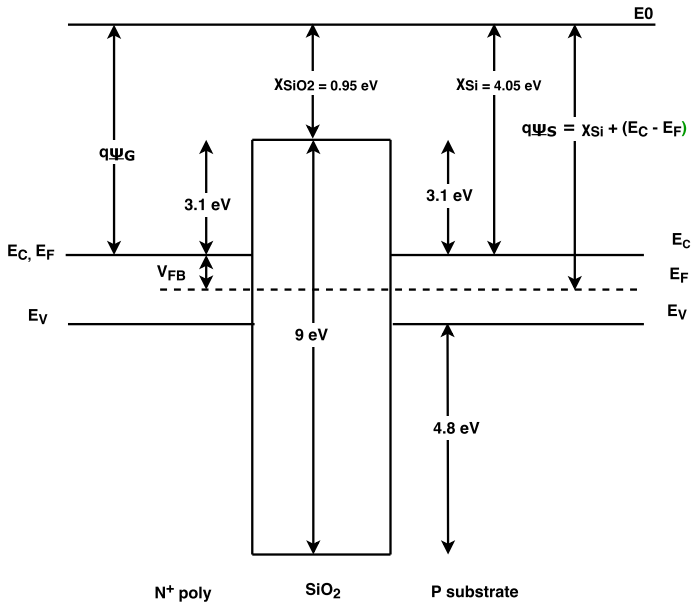


Figure 4.14: *Band energies for poly/SiO_2/P-substrate structure under the flat-band condition (V_G=V_{FB}). In this diagram the energy levels are reported as a function of the spatial dimension: the substrate is on the right side and the poly is on the left side*

When the gate voltage drops below V_{FB}, the accumulated negative charge is slowly removed and a depletion region starts to grow below the insulator. In this condition the capacitance drops until to reach its minimum when the depletion region does not expand any more. The MOS works in depletion (Figure 4.13). If V_G further decreases, holes will be attracted generating a layer of positive charge in the silicon surface (inversion phase). In general also this positive charge does not cross the insulator due to the energy barrier in the Si/SiO_2 interface.

To summarize, during the negative sweep the MOS works first in accumulation (maximum capacitance), then in depletion (the capacitance drops down) and to

conclude in inversion (the capacitance is the minimum). In general the curves reported in Figure 4.12 follows quite well these phases but a strong dependency by the sweep direction is evident. In positive sweeps the threshold voltage seems shifted towards lower values whereas in the negative it moves to the opposite direction. To generate the first shift the concentration of holes in the inversion layer should decrease faster than what expected. This can be caused by trapped holes in the insulator during the inversion phase. In this case indeed, the C-V characteristic would shift towards lower voltage as happens in the results got from the positive sweeps. The shift observed during the negative sweep instead, can be due to negative charge trapped in the insulator during the accumulation phase. In this case indeed, electrons on the silicon surface will be removed faster than what happens with a neutral oxide and the depletion will start earlier. The thresholds found with negative sweeps show that the negative trapped charge is higher in MOS18 (10^{12} cm^{-2}). When electrons are trapped in the insulator, part of them can recombine with old trapped holes reducing to zero the trapped holes concentration. Since the same happens when holes are trapped, the hysteresis can be reproduced several times always with the same values. Thanks to this property in regions where the gate contact is present, it is possible to place or extract charge from the insulator by means of direct or indirect voltage sweeps. However, this contact is not present everywhere on the detector backside and thus there is not a complete control of the trapped charge. As a consequence of this undesired charge, where its concentration is not negligible, the silicon surface could present a conductive channel of holes (in case of trapped-electrons) which may generate undesired shorts.

The insulator used to build the backside is an Oxide - Nitride - Oxide (ONO) grew by means of Chemical Vapor Deposition (CVD). Since the electron affinity of the nitride is higher (2.1 eV) than the one of the silicon oxide (0.95 eV), the nitride layer may act as a trap for charges injected in the insulator. It is known that the thickness of the oxide layers is very small, therefore it is possible that electrons and holes overcome the energy barrier of the Si/SiO_2 by tunneling. It leads to the though that small differences of oxide thickness in different wafers lead to different hysteresis as has been observed in the measurements.

The charge trapping effect in silicon nitrides of MONOS (Metal - Oxide - Nitride - Oxide - Silicon) devices is in general more complex and the trapped charge can be, as already discussed, both positive and negative. The effect has been extensively studied by White [54] who has developed the main theories about the charge storage

and transport in MONOS devices. The origin of the nitride traps are due to the existence of dangling bonds in silicon (SDB) which have three states of charge denoted as D^+, D^0 and $^-$. Traps in the D^+ state will contain positive charge (holes) and those in the D^- will contain negative charge (electrons). Traps in the D^0 are considered neutral and thus can be occupied by an electron or a hole. More details about these theories can be found in [55].

During the measurements it has been observed that the shifts depend somehow by the magnitude of the initial bias. Generally they increase when also the initial gate bias increases suggesting that more charge is induced in the insulator. It has also been observed that increasing the initial bias, the threshold shift presents a saturation.

TCAD simulations with negative trapped charge in the backside oxide confirms the generation of a inversion layer in the whole area of the backside which reaches the cut line of silicon.

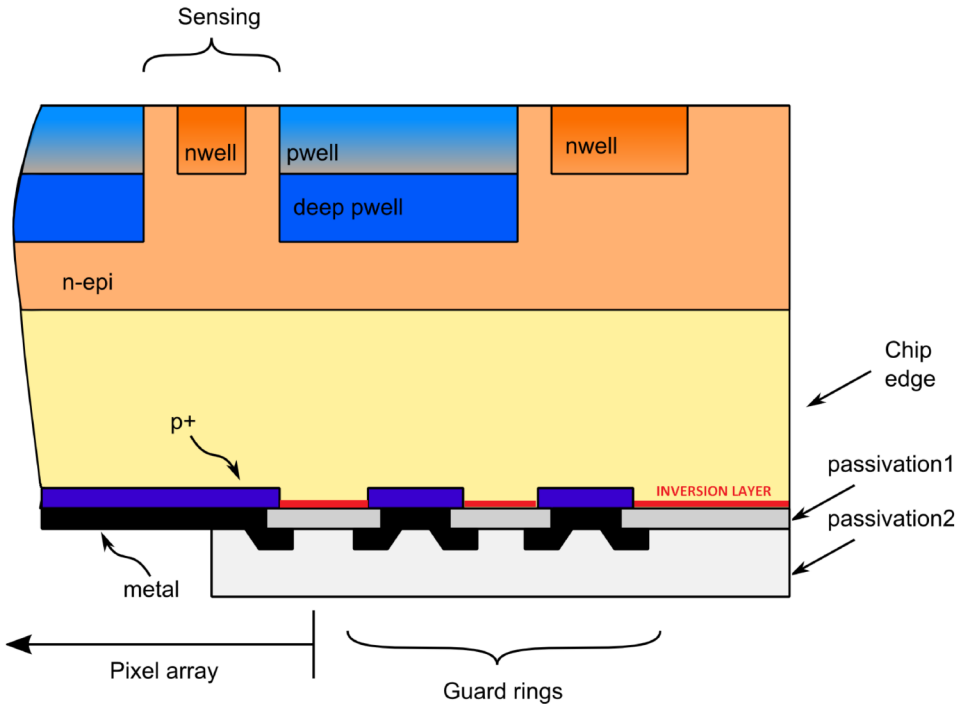


Figure 4.15: *Cross section of the backside. The passivated film is shown and also the inversion layer of holes which causes the short circuit between the rings of the guard-ring structure.*

Due to the negative charge, some undesired effects are expected in the guard-rings. If the inversion layer is between the rings (see Figure 4.15) it can create shorts which

will unavoidable affect the breakdown and the leakage behaviour of the devices. In this condition the test diodes should behave in the same way independently by the number of rings built on the backside. All these considerations leads to think that the devices built on wafer 19 will have a better performance than those built on wafer 18.

To confirm the hypothesis of trapped charge, a dedicated irradiation test by means of X rays up to 10 Mrad has been done in Padova. Irradiation in fact, introduce positive charge in the backside oxide which can compensate the effects of trapped-electrons and enhance the effects of trapped-holes.

Since the injection of electrons from the substrate to the nitride layer is by tunneling, also variations of few nm may be relevant. A TEM (Transmission Electron Microscopy) analysis done by the foundry confirmed that the oxide built on wafer 18 has an unexpected thickness and also an aberration in the interface with silicon. However, the process used for the production of wafer 19 is well known and can be used to fabricate new wafers trying to overcome the limitations so far discussed by simply removing the nitride layer or by using a thicker oxide which should not change the properties of the insulator.

Similar effects have been observed in memories based on nano-crystals where insulators are fabricated by means thermal oxidation [56][57]. Focused studies about the trapped charge by means of deep-level transient spectroscopy (DLTS) and discharging current transient spectroscopy (DCTS) on polysilicon/oxide/nitride/oxide (SONOS) insulators used in flash memories are discussed in [58], [59] and [60].

4.2.2 Characterization of the test diodes

Eight different simple p^+/n-sub diodes have been implemented in the test chip. As explained in Chapter 2, these devices differ by the contact realized on the backside and share the same terminal on the topside. For this reason the samples used for the characterization have been placed on the test board bottom up, as already shown in Figure 4.10. In order to highlight the important dependencies, the results shown in this section have been divided into two groups based on the two main categories of diodes. *Group A* contains diodes with the same number of rings (10 rings) but different pitch (GRP). *Group B* contains diodes with the same pitch (6 μm) but different number of rings (GRN). For the measurements the samples have been connected to the board by means of a conductive epoxy glue so that the n-terminal can be reached by means of a connector. For what concern the p^+ terminals, they have been connected to the test board through wire bonding as shown in Figure 4.16. The main parameters to measure during the characterization are essentially currents and capacitances under different backside voltages. So I-V curves have been extensively used to study the leakage of the devices and to identify the best guard-ring structure which allows to get the best performance. The depletion of the diodes has been studied by means of the common C-V characteristic.

At the end of this section results from X-rays irradiation tests are discussed.

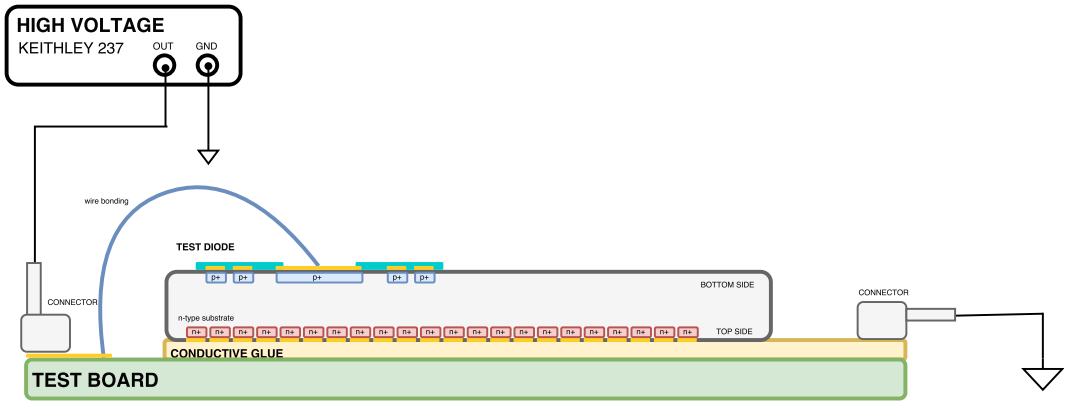


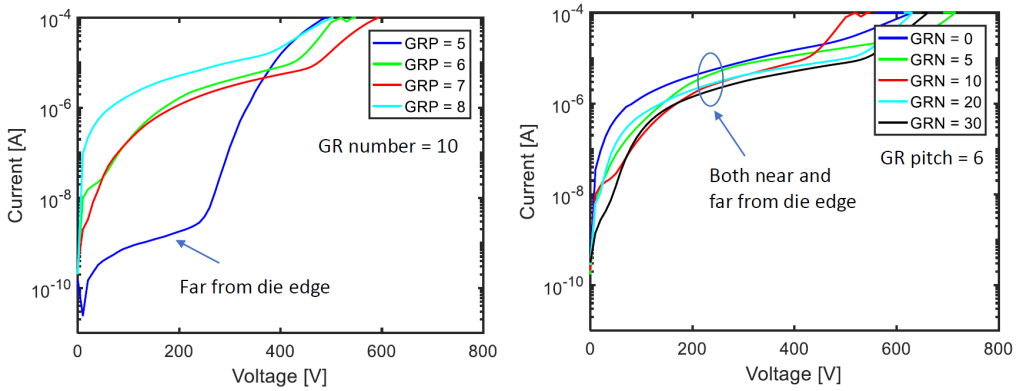
Figure 4.16: *Scheme of the setup used to measure leakage current in the test diodes.*

Measurements of leakage current

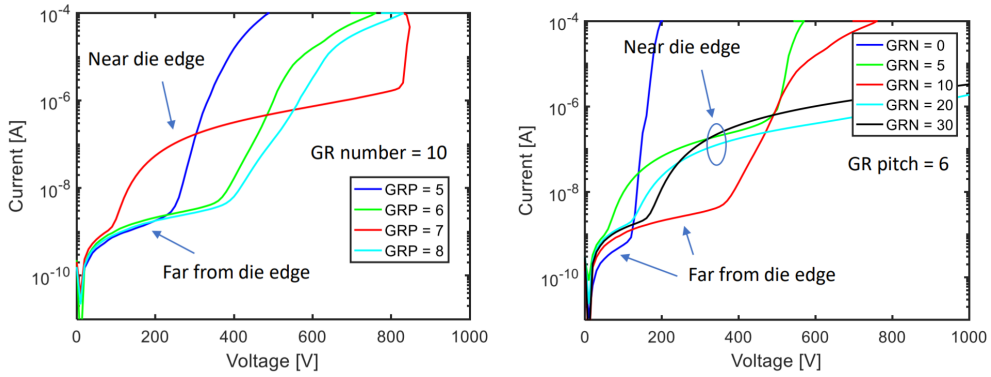
The leakage current has been measured in diodes built on wafer 18 and 19. The current has been measured for different backside voltages (V_{bck}) by following the scheme of Figure 4.16. The common nwell terminal has been connected to ground by means of the connector placed on the test board.

The HV is supplied by the Agilent 4156 (a semiconductor parameter analyser). It is also used to measure the current with very high precision. The measurement has been carried out by measuring the leakage current for V_{bck} voltage among 0 and a maximum voltage fixed by a compliance of 10 mA. Figure 4.17 resumes the I-V characteristic obtained at room temperature by keeping all the diodes in the dark. The leakage current of samples from wafer 18 increases rapidly up to 10 μA starting from small voltages independently by the number of rings and pitch used. Only for a diode from group A and located far from the die edge (GRP5) the current is much lower and in the order of tens nA up to 250 V. Apparently there is no dependency by the number of rings used to built the guard-rings. Also the dependency by the distance from the die edge is very weak because visible only in one diode. On the contrary in samples from wafer 19, it is possible to reach 200 V with a leakage current of units of nA which is considered low for a 300 μm thick sensor. Figure 4.17b shows that in these samples, the breakdown increases with the number of rings so that structures with 20 and 30 rings can sustain voltages up to 1000 V. Also the dependency by the distance between the diode and the die edge is more visible. In fact at nominal bias ($\sim$160 V), diodes built close to the die edge has a moderate current ($<$ 1 μA). Contrary in diodes placed further, the leakage is significantly much lower ($\sim$ 2 nA). Also in this case, as happens with diodes from wafer 18, the leakage increases up to 100 μA but very slowly.

Results from samples belonging to wafer 18 and 19 are very different and this is explained by the strong correlation between insulator charge and electrical behaviour of the guard-rings as has been explained during the characterization of the MOS capacitor. As expected from the characterization of the backside insulator due to the high concentration of negative charge, all the diodes from wafer 18 behave in the same way independently by the topology of guard-ring used on the backside. Contrary in samples from wafer 19, there is a dependency by the topology and in general those samples have a better performance because they can sustain higher voltages with a much lower leakage current.



(a) *I-V of samples from wafer 18. Curves from group A on the left and from group B on the right.*



(b) *I-V of samples from wafer 19. Curves from group A on the left and from group B on the right.*

Figure 4.17: *I-V characteristic from samples from wafer 18 (a) and 19 (b). The curves have been divided into two categories: on the left all the diodes with the same number of rings (10) and on the right diodes with the same pitch (6µm)*

Effects of X-rays radiation

Results from the backside characterization highlighted the presence of undesired negative oxide-trapped charge which leads to the guard ring failure in all the test diodes. To confirm that this effect is due to the trapped charge, dedicated irradiation test has been planned. Ionizing radiation can induce significant positive charge in oxides and insulators [61]. Although this charge generally leads the device to degradation and sometimes also failure, in this case it can be used to counterbalance the trapped-electrons and enhance the trapped-holes observed during the characterization of the

MOS capacitor. In general the higher is the radiation dose delivered on the device, the higher is also the positive charge induced in the insulator. In this condition, the probability of having recombination effects between the trapped negative charge and the new trapped holes increases. From this point of view the radiation damage should allows the device recovery allowing to increase the breakdown voltage of the test diodes.

The irradiation tests have been carried out at the INFN of Padova by means of the X-ray irradiation system depicted in Figure 4.18. The facility is the RP-149 Semiconductor Irradiation System from Seifert equipped with a X-ray tube based on a tungsten anode. The figure shows the tube located inside the cabinet where it is also installed a motorized chuck which can move the samples in x/y/z with an fine accuracy of 30 μm [62]. The X-ray spectrum of the machine, depicted in Figure 4.19, consists of the bremsstrahlung spectrum with the characteristic twelve radiation lines of tungsten among 8.3 and 11.7 keV.

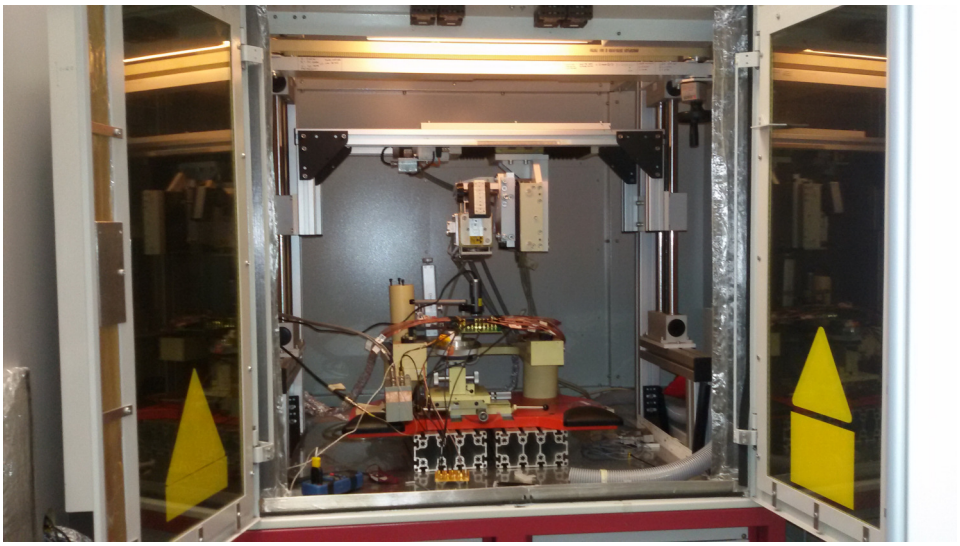


Figure 4.18: *X-ray radiation source used for studies of radiation effects on the test structures.*

The dose rate (D_R) of the facility has been measured by means of a square silicon calibrated diode and can be determined as follows:

$$D_R = \frac{C \times I_X}{q \times E_{e-h} \times V \times \rho} \tag{4.2}$$

where C is a calibration constant, I_X is the current induced by the radiation, q is the electron charge, E_{e-h}=3.6 eV is the energy required to create an electron-hole

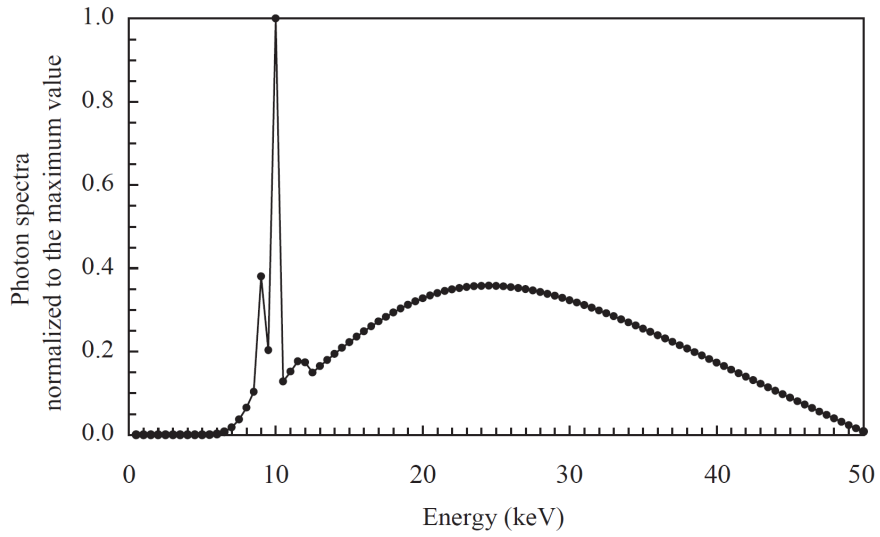


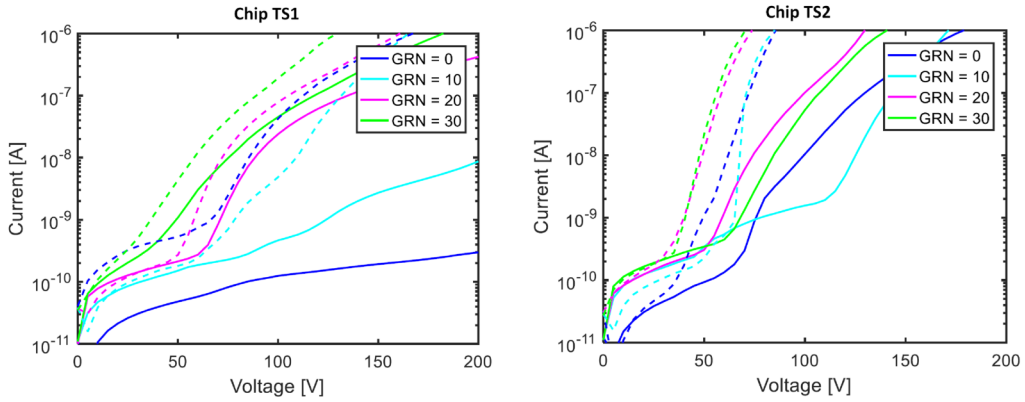
Figure 4.19: *Normalized X-ray spectrum from [62].*

pair and ρ is the silicon density. The dose rate depends by the position but the average value of dose rate in silicon is $\sim$60 rad/s.

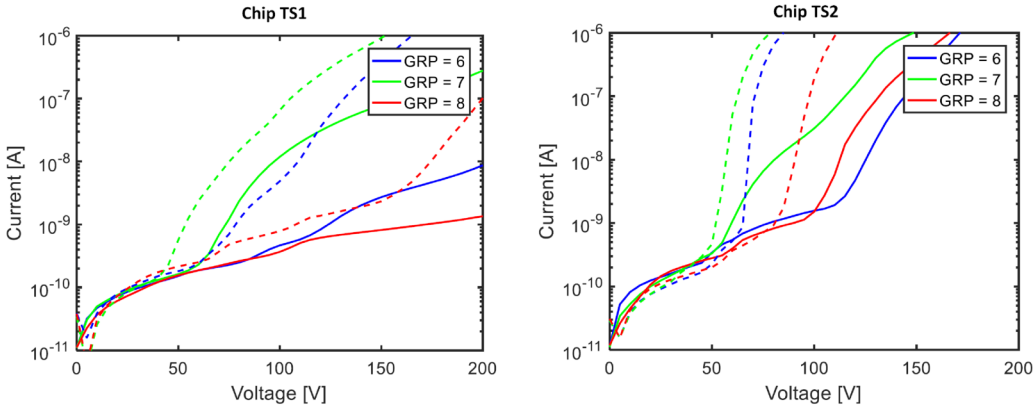
Two samples (TS1 and TS2) from wafer 24 have been exposed to two different level of radiation. At the beginning they have been irradiated for about 5 hours in order to reach a total dose of 1 Mrad. Before and after the irradiation the diodes has been characterized by means of the I-V curves and the MOS capacitor by means of the classic C-V characteristic. Results after the irradiation have been summarized in groups and are reported in Figure 4.20. In general before the irradiation (dash lines in Figure 4.20a) the two samples are similar: the breakdown voltage is around 50 V and the measured leakage with this bias is in the order of 400 pA. It is not observed any dependency by the number of guard-rings but the results suggest that higher is the pitch used, slightly higher is the breakdown voltage.

After 1 Mrad of irradiation, the diodes have in general a better performance. Indeed, the breakdown voltage moves towards higher values. However, it is still not clear what is the benefit in using more guard-rings because most probably the effect of the trapped charge in the oxide is still present.

The MOS capacitor has been characterized before and after the irradiation by means of the same measurement described in Section 4.2.1. The results, shown in Figure 4.21, show that in both samples the hysteresis is still present after the irradiation. As expected, the irradiation produces a shift of the threshold voltage



(a) *Results from diodes from group A of TS1 (on the left) and TS2 (on the right).*



(b) *Results from diodes from group B of TS1 (on the left) and TS2 (on the right).*

Figure 4.20: *First run of irradiation of two samples TS1 and TS2 from wafer 24. The I-V curves of all the backside diodes are divided into two groups. Group A (4.20a) collects diodes with 6 µm pitch and different guard ring number; Group B (4.20b) contains diodes with 10 rings and different pitch. Results from samples TS1 and TS2 are reported on the left and right side respectively. Dash line corresponds to the pre-irradiation characteristic and solid line corresponds to the characteristic after 1 Mrad irradiation with X-rays.*

towards lower values suggesting that positive charge has been induced in the ONO insulator. This is more evident in fact, in the positive sweep because this extra positive charge helps to increase the number of electrons in the region below the gate and this turns in a lower threshold voltage. The shift generated by radiation is present also in the curve obtained with the negative sweep. However, the effect here is significantly much weaker most probably because the radiation level was not sufficient to compensate the negative trapped charge in the oxide. For this reason a

second irradiation run has been done with the same samples to reach a total dose of 10 Mrad. The results (Figure 4.21) remarks the same shifts observed with 1 Mrad but, as expected, in this case the effect is more evident also in the results collected from the negative sweeps. Table 4.1 and 4.2 resumes the shifted voltages before and after the irradiation.

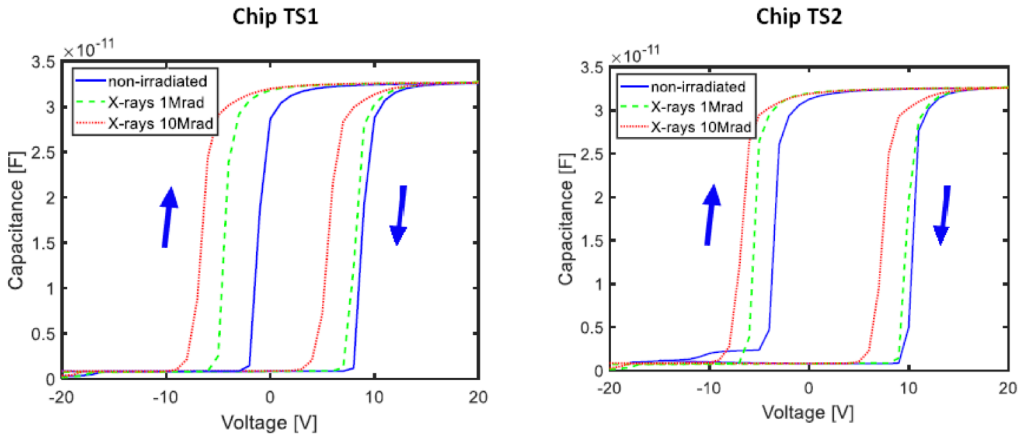


Figure 4.21: *C-V characteristic of two samples from wafer 24 before (blue line) and after the irradiation up to 1 Mrad (green line) and 10 Mrad (red line). Arrays indicate the sweep direction used in the measurement.*

Parameter	Before irradiation	after 1 Mrad	after 10 Mrad
V_{TH}^{+}	-2 V	-5 V	-7.5 V
V_{FB}^{+}	0 V	-4 V	-5 V
V_{FB}^{+} - V_{TH}^{+}	2 V	1 V	2 V
V_{TH}^{-}	8.3 V	8 V	5.5 V
V_{FB}^{-}	10 V	9.5 V	7.5 V
V_{FB}^{-} - V_{TH}^{-}	1.7 V	1.5 V	2 V
V_{TH}^{-} - V_{TH}^{+}	10.3 V	13 V	13 V

Table 4.1: *Radiation effects on threshold and band-flat voltage of the sample TS1. Positive and negative signs are used to indicate that the parameter refers to the positive or negative sweep.*

The effect of the 10 Mrad irradiation is the shift of the hysteresis curve of ∼5 V which is not enough to remove completely the undesired charge from the insulator but it is enough to debilitate the undesired inversion layer and thus improving the

Parameter	Before irradiation	after 1 Mrad	after 10 Mrad
$\mathbf{V}_{TH}^{+}$	-4 V	-6 V	-7.2 V
$\mathbf{V}_{FB}^{+}$	-1.5 V	-4 V	-4.8 V
$\mathbf{V}_{FB}^{+}$ - $\mathbf{V}_{TH}^{+}$	2.5 V	2 V	2.5 V
$\mathbf{V}_{TH}^{-}$	10 V	9.7 V	7 V
$\mathbf{V}_{FB}^{-}$	12 V	-13.2 V	11 V
$\mathbf{V}_{FB}^{-}$ - $\mathbf{V}_{TH}^{-}$	2 V	2.5 V	3 V
$\mathbf{V}_{TH}^{-}$ - $\mathbf{V}_{TH}^{+}$	14 V	15.7 V	14.2 V

Table 4.2: *Radiation effects on threshold and band-flat voltage of the sample TS2. Positive and negative signs are used to indicate that the parameter refers to the positive or negative sweep.*

performance of the devices. The I-V curves obtained after 10 Mrad indeed shows a clear improvement in terms of breakdown voltage and leakage current. Figure 4.22 shows a comparison between four diodes from TS1 and TS2. After 10 Mrad in all diodes it is visible the same effect: from the one hand the breakdown voltage increases allowing to sustain higher voltages with a lower leakage while from the other hand the leakage, as expected, increases as effect of the irradiation damage. However, it is in the order of 50 nA/cm^3 which is still low for a 300 μm sensor. The best performance is reached for diodes with 10 rings and pitch of 8 and 6 μm where the measured leakage in condition of full depletion (-90 V) is 1 nA.

To resume, I-V curves after radiation show better performances since the breakdown generally increases. From the C-V measurements on the MOS capacitor, a shift of the characteristic towards low voltages has been observed: this confirms that the trapped charge in the oxide affect the performance of the device. In general we can say that the hypothesis that the early breakdown observed is due to negative and positive charge in the oxide is validated by the measurements but the 10 Mrad irradiation is not enough to definitely contrast the negative charge observed during the negative voltage sweep. For this reason, in the tested samples it is possible to find thin conductive channels which connect the junctions up to the cut-line of silicon causing early breakdown.

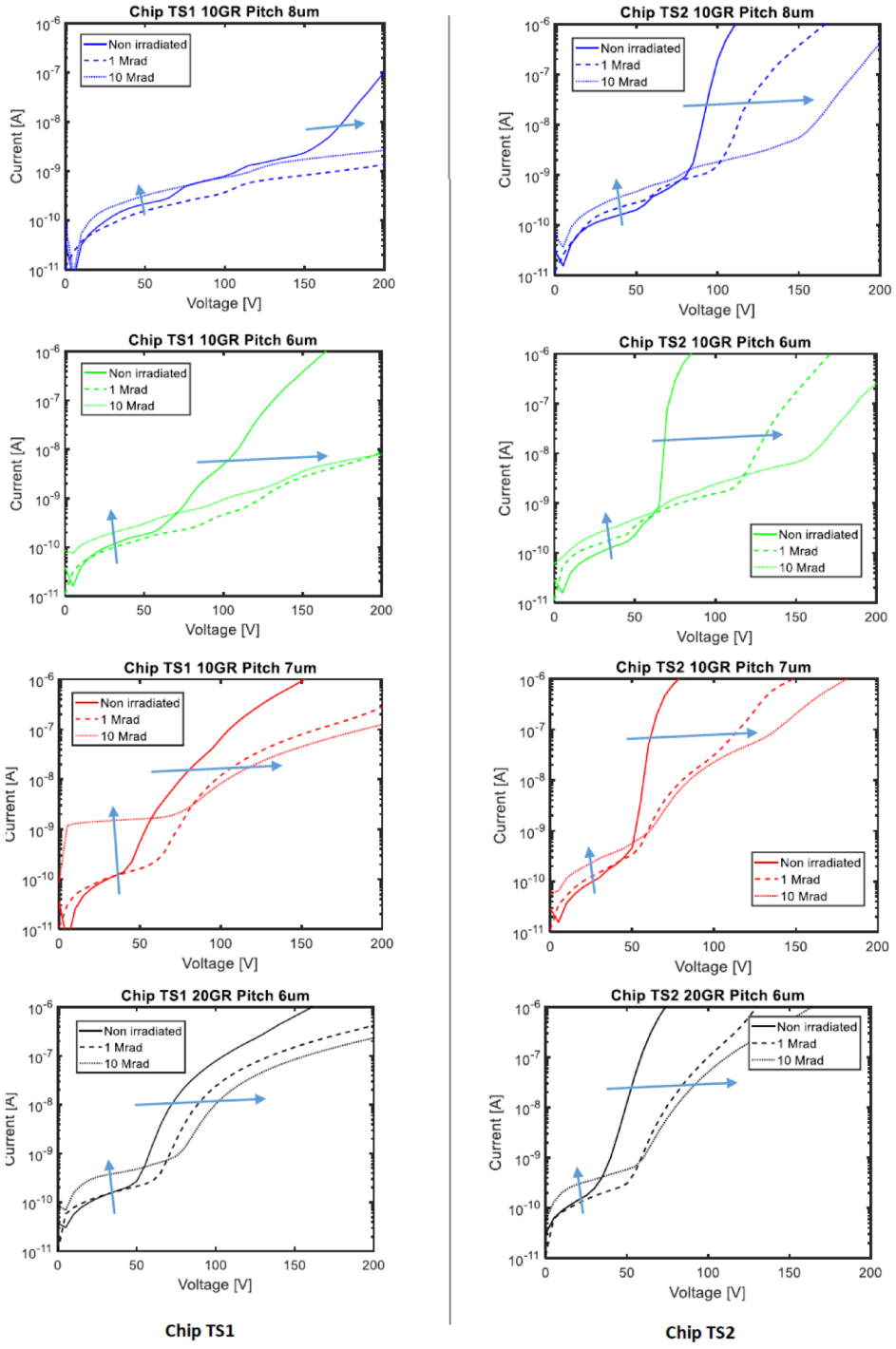


Figure 4.22: *I-V curves of backside diodes with 2 different doses of radiation: 1 Mrad and 10 Mrad. On the left the results from the sample TS1; On the right results from sample TS2. In each sample diodes with different number of rings and pitch have been tested.*

4.2.3 Characterization of the test matrices

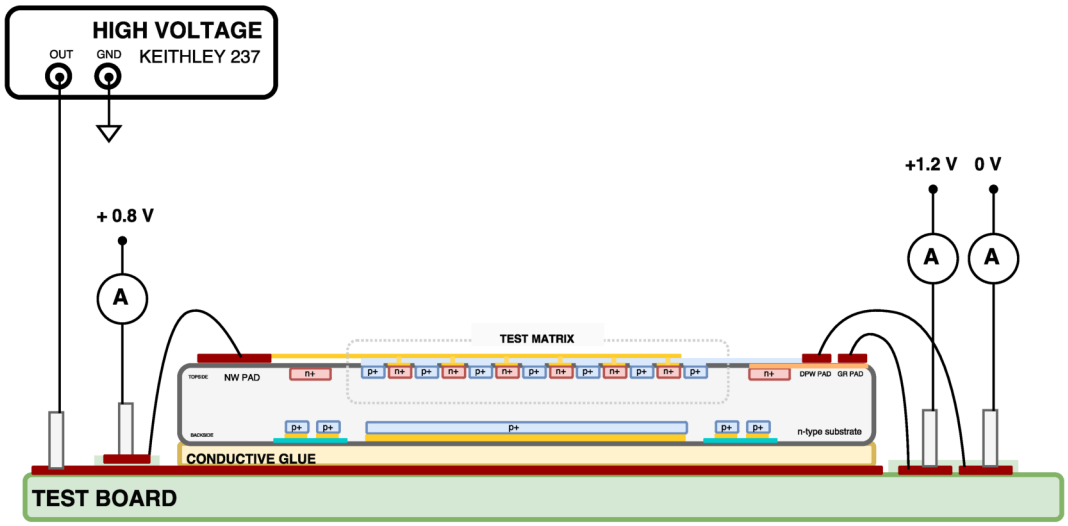


Figure 4.23: *Setup used for the I-V measurements of the test matrices*

Three matrices with a different pixel size have been built on the test chip. The pixels sizes are 10 μm, 25 μm and 50 μm. The intent of those dimensions is studying the effects of the pixel size in the depletion of the device. The matrices share the backside terminal for the p^+ polarization which is surrounded by a single guard-ring. The polarization of this part is done through the test board as shown in Figure 4.23. On the top side, the collector terminals of each matrix are shorted and connected to a dedicated PAD. Around the matrices a guard-ring (GR) has been built to protect the channels against undesired currents coming from the chip edge. Also the polarization of this GR is done through a dedicated PAD. Even if the test matrices do not contain any circuitry on board, they have been built with the deep-pwell required by the CMOS circuitry. The deep-pwell can be biased by means of a PAD of the test chip. Thanks to these additional PADs, not foreseen in MATISSE, here it is possible to access also the collector node to study in detail what happens at the input of the pixels.

Measurement of leakage current

The leakage of the matrices has been studied by means of the I-V curves as for the test diodes. The measurement has been carried out by using the setup depicted in Figure 4.23. All the PADs has been connected to a fixed voltage: the guard-ring is

connected to 1.2 V, the deep-pwell to ground and the nwell is connected to 0.8 V in order to emulate the expected values of MATISSE.

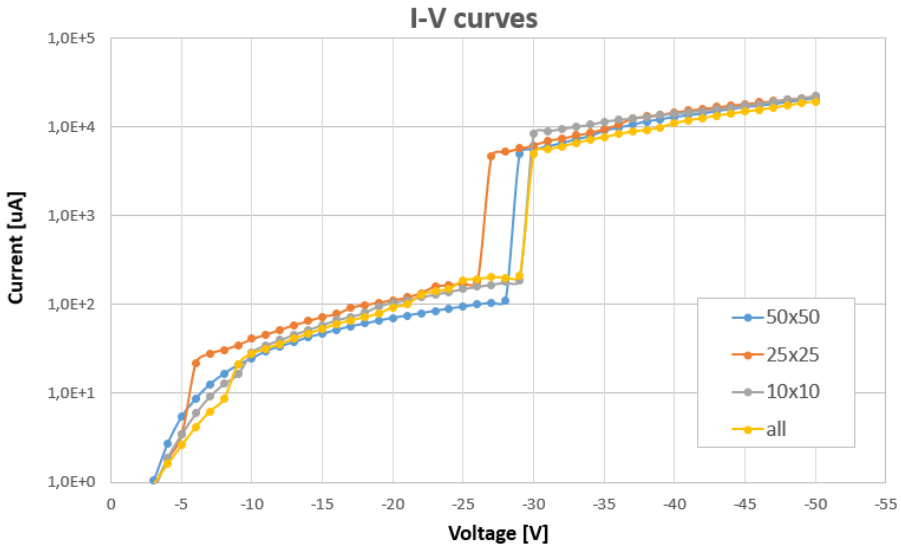


Figure 4.24: *I-V curves of matrices from wafer 24. The breakdown is around 30 V.*

Figure 4.24 shows the I-V curves of a sample from wafer 24. The breakdown is around 30 V independently of the pixel size. The leakage at very low voltage is also significantly high (tens of μA).

Studies of full depletion

The test matrices allow to study what happens in each layer used to built the device. For this reason, a dedicated measurement has been carried out with the intent of monitoring the currents which flow in the sensor when the backside voltage decreases. The setup used for the measurement follows the same scheme of Figure 4.23. The measurement consists in monitoring the current collected by the nwell I_{NW}, the one flowing through the guard-rings I_{GR}, the current from the deep pweel I_{DPW} and finally the current flowing through the backside terminal I_{BCK}. All these currents are collected in Figure 4.25. The current I_{NW} is the sum of the current collected by the three matrices. The negative sign has been assigned to currents which comes out from a terminal. The measurement has been carried out with a test structure from wafer 24, at room temperature and in the dark.

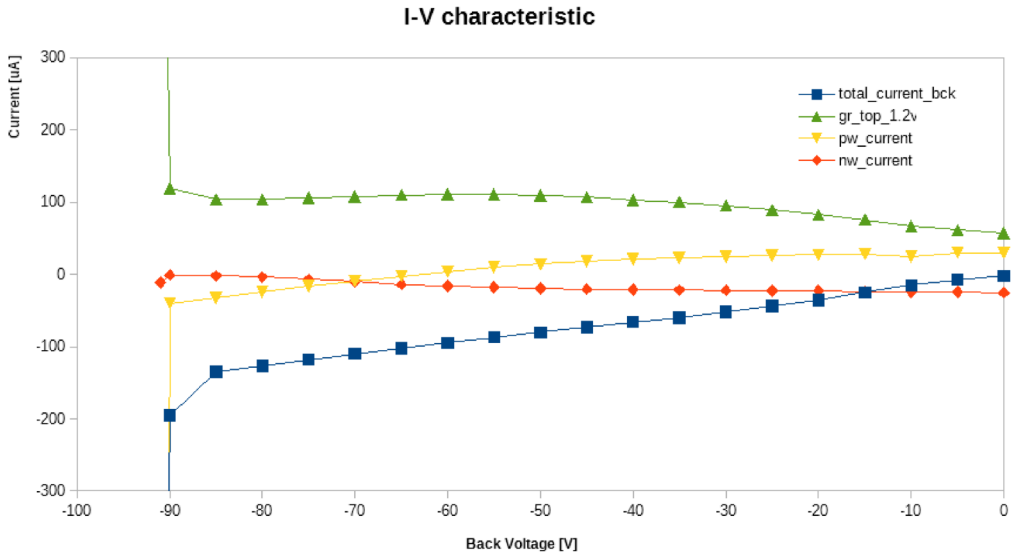


Figure 4.25: *Currents flowing in the test matrices for different voltages applied at the backside*

When V_{BCK} is zero, there is no current flowing through the backside and all the currents flow on the top. A current of 60 μA flows through the guard-ring and is divided between the nwell and the deep-pwell. This current is generated by the voltage drop of $\sim$400 mV between nwell and guard-ring, and by the resistive path on the topside. In this situation each pixel receives a constant input current which, if some electronics were be implemented on board, would lead to saturation all the channels. When V_{BCK} decreases, I_{NW} slowly increases up to zero around -85 V. This can be considered an indicator of full depletion of the device. However at -90 V there is an unexpected early breakdown because the current suddenly increases up to reach the compliance of the voltage source. It is important to notice that during the measurement, the current flowing in the guard-ring is always high ($\sim$ 90 μA). This means that the current flowing through the chip edge is so high most probably because of its small distance from the device. Since the depletion voltage is lower than the expected (-150 V) it is assumed that the doping concentration of the substrate of wafer 24 is lower that the expected value. Moreover the trend of I_{DPW} shows an unexpected early punch-through around -50 V. For higher values indeed, this current increases rapidly and can even becomes positive.

As done for the test diodes, the depletion has been studied also by means of the C-V curve in a sample from wafer 19. Since the connection with the backside is

critical, for this measurement the sample has been glued to the test board bottom up creating a short between the PADs of nwell, deep-pwell and guard-ring. The terminal on the top has been connected to the HV supplier by means of a probe-station needle whereas the shorted contacts have been connected to ground. Also in this case the HV source used is the Keithley 237 and the RLC meter is the HP4284A. Figure 4.26 reports the C-V characteristic obtained by the measurement.

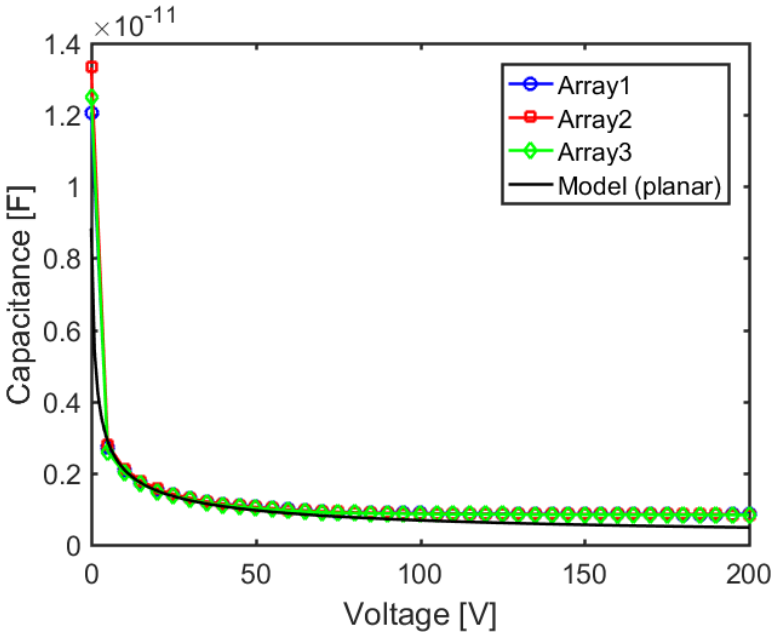


Figure 4.26: *C-V characteristic of the three matrices of the test chip from wafer 19.*

The results show that the three matrices behaves more or less in the same way. The capacitance at 0 V is 14 pF and suddenly decreases after few volts. The minimum capacitance is 1 pF and is reached around ∼140 V. Therefore, this is assumed to be the depletion voltage of the sample. The results are also compared with a model of an asymmetrical junction p^+/n-sub with a doping concentration of 2.4×10^{12} cm^{-3} and area of 1.25 mm × 1.25 mm. The model fits quite well the data up to 30 V and then is different most probably because the guard-ring built on the backside starts to work also at low voltages.

Figure 4.27 shows the trend of $1/C^2$ commonly used to estimate the effective doping concentration of the substrate. Also in this case the collected data have been compared with the model of an asymmetrical junction with the expected doping concentration of 2.4×10^{12} cm^{-3}.

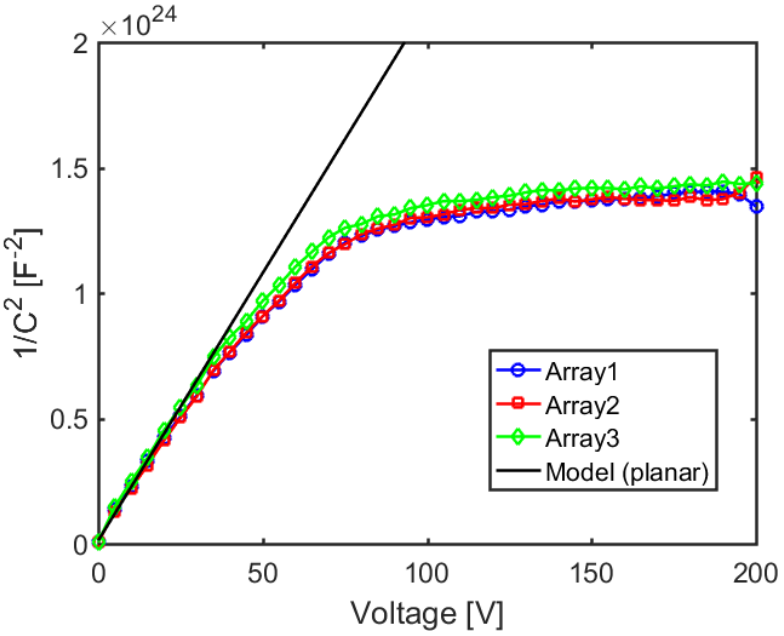


Figure 4.27: *$1/C^2$ trend used to estimate the effective doping concentration of the wafer.*

Since the model fits quite well the results, it is assumed that the doping concentration of the wafer is $2.4 \times 10^{12}\text{cm}^{-3}$. This result is in good agreement with the formula 4.3 used to estimate the depletion voltage of a sensor made by an asymmetric junction. In the formula W is the sensor thickness, q is the electron charge, N_{eff} is the effective doping concentration, ε_{Si} is dielectric constant of silicon and ε_0 is the vacuum dielectric constant.

$$V_{dep} = \frac{W^2 \times q \times N_{eff}}{2 \times \varepsilon_{Si} \times \varepsilon_0} \tag{4.3}$$

By using the expected doping concentration, the depletion of the full sensor should be 165 V. This value is in good agreement with the results obtained from the C-V curves.

4.3 Characterization of MATISSE

MATISSE, as all the detectors from the monolithic category, is composed by sensor and electronics implemented in the same silicon wafer. During the ASIC design, an effort has been done to be able to test the electronics independently of the sensor. This was made possible by the generation of internal pulses at the input of each pixel which emulates the effect of real signals coming from the sensor. Thanks to this feature, the characterization of MATISSE has been divided into three steps. First, the p^+/n-sub diode has been characterized to study depletion, punch through and leakage current. Results from this phase can be compared with results obtained from the test structures built on the same wafer. The second step is the independent characterization of the readout electronics by means of the injection of charge at the input of each channel. In this phase, even if the sensor is not used, it is very important to work in full depletion in order to reduce the effects of leakage current in the measurement. At the end, the complete detector is tested with the use of monochromatic light sources which from one side, allows seeing the performance of MATISSE as an X-rays detector and from the other side, allow also to get the calibration of the whole system.

The following sections have been divided by following these steps. Results obtained with the test diodes shown that samples built on wafer 19 have better performance in terms of depletion than the other wafers. For this reason, all the results presented hereafter have been obtained with samples from this wafer. When the sample will come from a different wafer, it will be indicated.

4.3.1 Characterization of the pn junction

Studies of full depletion

The tools used for the studies of full depletion and leakage current are again C-V and I-V curves. Both in diodes and matrices from the test structures, the C-V characteristic has been obtained by measuring the capacitance between the p^+ terminal on the bottom side and the n^+ terminal on the top. However, in MATISSE due to their interconnection with the very front-end, the n^+ terminal of each pixel can not be reached in any way. For this reason, the capacitance has been measured between the deep-pwell and the p^+ terminal on the backside. The simplest way to

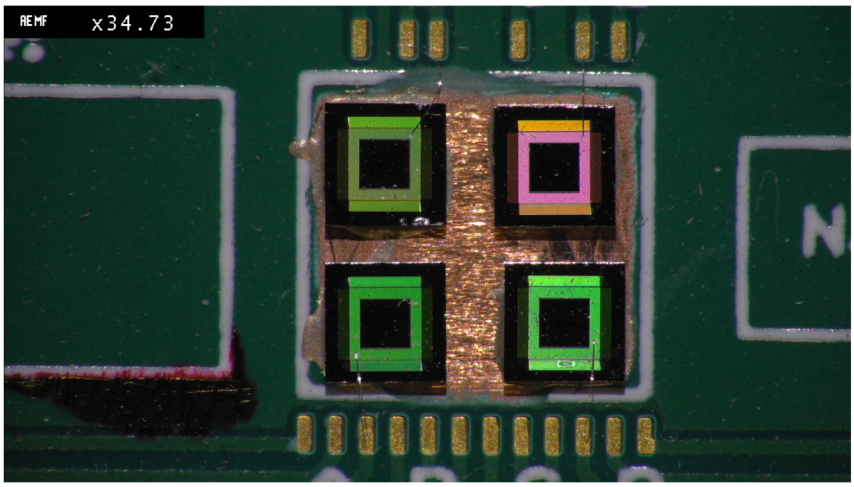


Figure 4.28: *Four samples glued bottom up to a test board. In each sample wire bonding is used to connect the p^+ terminal and a PAD of the test board.*

carry the measurement out is placing a sample on a test board bottom up by means of the conductive epoxy glue. In such a way, all the pads are shorted and connected to a fixed voltage (ground) and the backside can be easily connected from the top. During the characterization of the test structures, it has been observed that the risk of having trapped charge in the oxide is high. For this reason, it was important to contact the backside with high accuracy avoiding the use of conductive epoxy glue on the insulators. The best way to do this operation is through wire-bonding. Figure 4.28 shows a picture of four samples glued to a test board bottom up where the backside is connected by means of this technique.

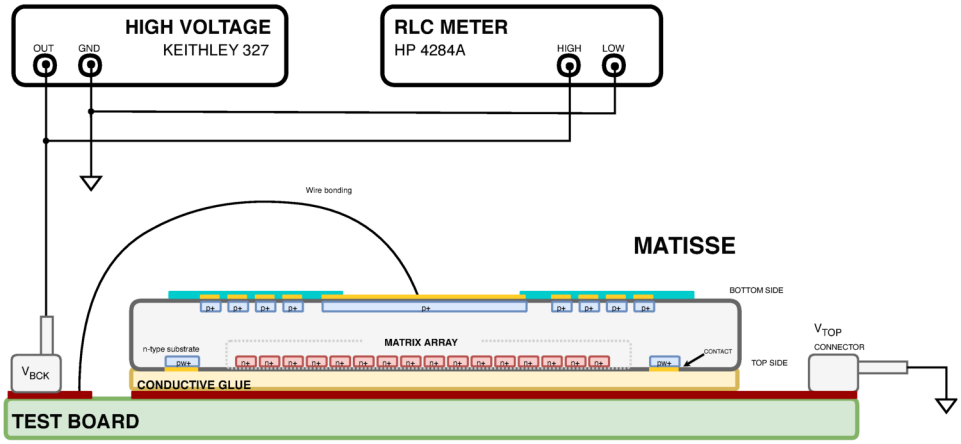


Figure 4.29: *Setup used to measure the capacitance and leakage current of MATISSE*

During the measurements, voltages and currents have been measured by means of the HV Keithley 237 whereas the capacitance has been measured with the RLC meter HP4284A following the scheme depicted in Figure 4.29.

The C-V characteristic reported in Figure 4.30 shows that the measured capacitance decreases rapidly and reaches a minimum value of 2.8 pF which is compatible with the minimum measured in the test matrices (1 pF) taking into account the different diode size. It is well known that the C-V characteristic can be used to determine the depletion voltage of pn junctions [63]. However, from the C-V obtained is not clear what is the exact value of V_{BCK} which leads the capacitance to the minimum. It is anyhow reasonable to consider that the depletion voltage is higher than 80 V.

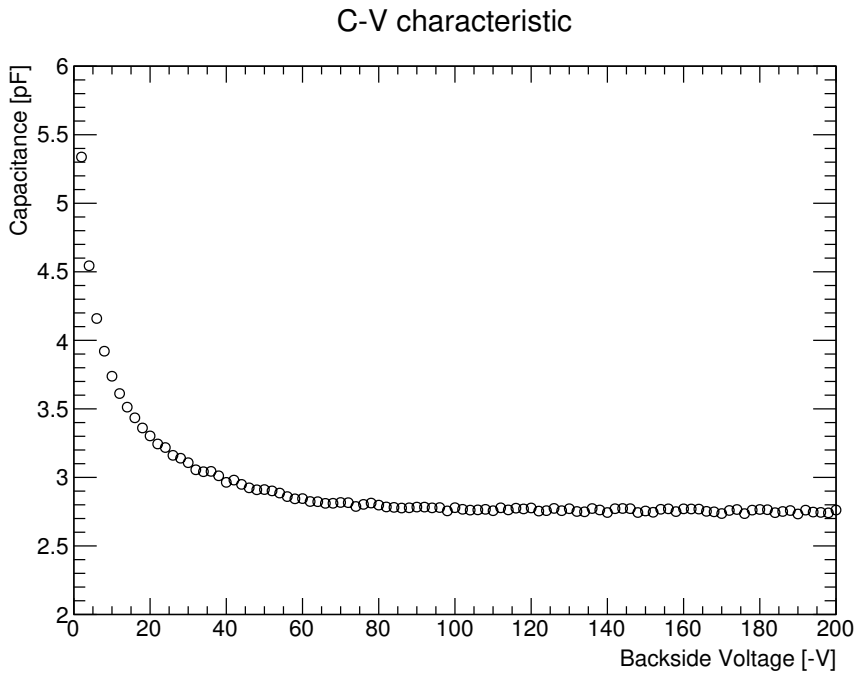


Figure 4.30: *Capacitance over backside voltage of the monolithic sensor placed bottom up on the test board. The minimum capacitance is reached for V_{BCK} values higher than 80 V.*

The $1/C^2$ trend reported in Figure 4.31 has been compared with an ideal one-sided p^+-n junction with an area of 1.25 mm$\times$1.25 mm and doping concentration equal to 2.4×10^{12} cm^{-3}. The measurement follows quite well the model only for low voltages and then suddenly increases much slower in the same way observed in the test matrices. Also in this case, the effect is attributed to the guard-rings on the backside which works also at low voltages. By using the linear fit at low voltage

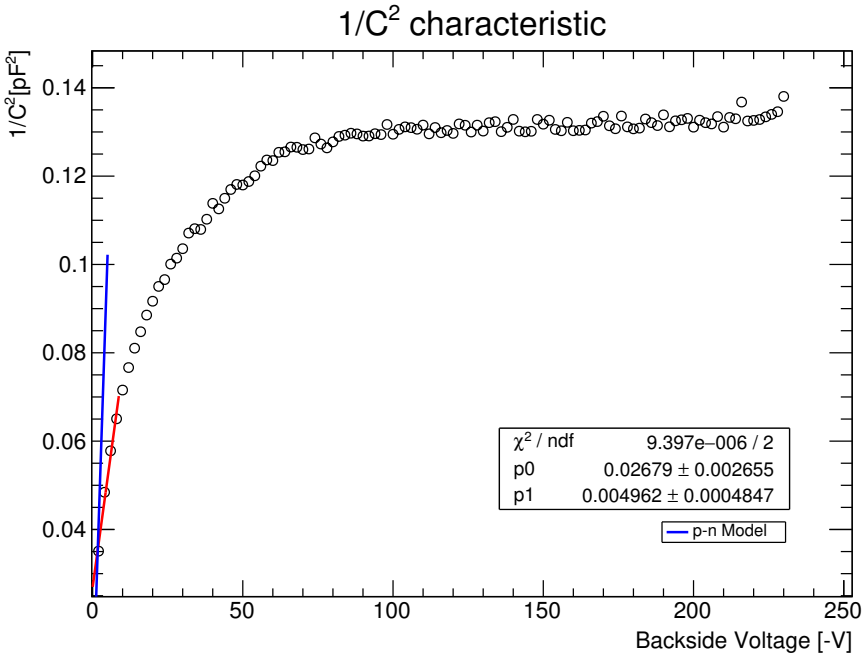
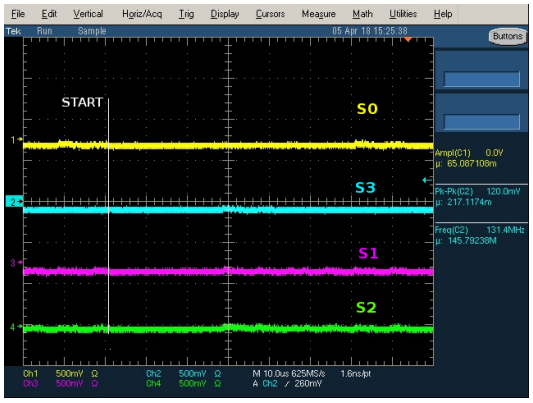


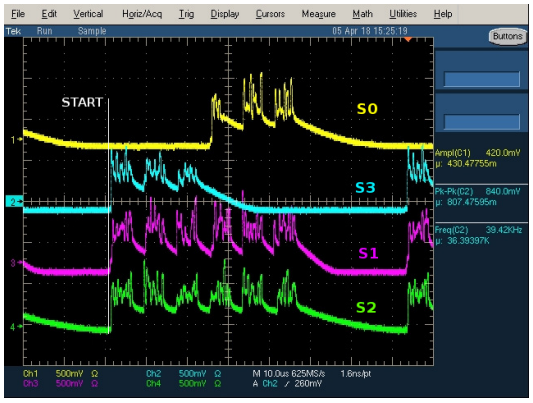
Figure 4.31: *The 1/C^2 over the backside voltage compared with an asymmetric p-n model (blue line).*

values, the effective doping concentration of $\sim 1 \times 10^{12}$ cm^{-3} has been obtained. This number is the same order of magnitude from what expected.

This measurement is a good tool to evaluate the substrate full depletion voltage but it can not be used to understand what happens in the epitaxial layer. However, this information can be obtained from the readout electronics. It has been observed indeed, that when low voltages are applied at the backside, the channels receive at the input a constant current generated by the presence of free charges on the silicon surface and by voltage drops. Inevitably this causes the saturation of the channels. The only way to avoid the saturation is removing the free charges located in the silicon surface and this happens only when the depletion region reaches the maximum extension of 300 μm. Figure 4.32 shows the four analog outputs sent by the detector at different backside voltages. For the measurement, the integration time has been set to $\sim$10 μs and the sample has been kept in the dark in order to avoid the charge collection generated by light photons. The analog data generated by a sector is made by the voltage outputs of all the 144 pixels which are read serially by means of a vertical and a horizontal clock. The starting point of the readout procedure is indicated by a white line. At 100 V, all the outputs are zero. This

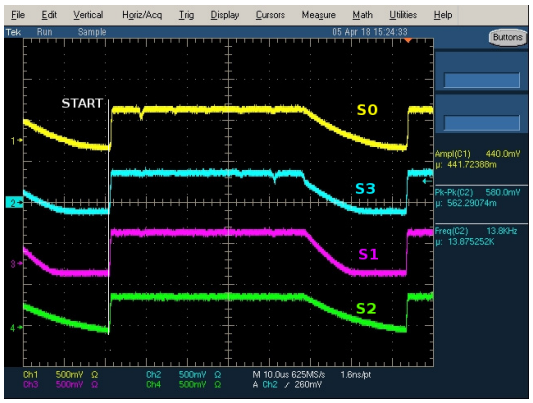


(a) $|V_{BCK}| = 100\ V$

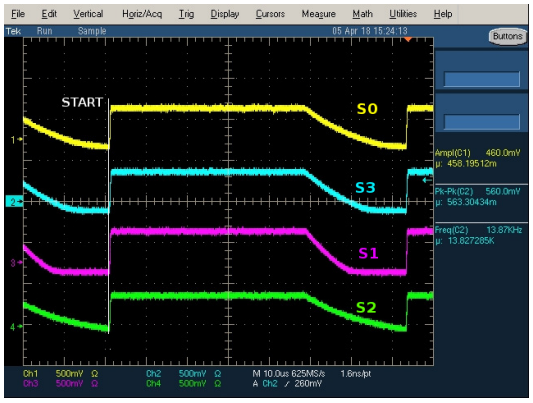


(b) $|V_{BCK}| = 110\ V$

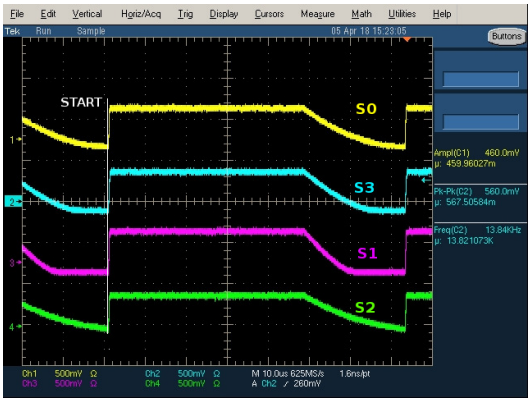
(c) $|V_{BCK}| = 120\ V$



(d) $|V_{BCK}| = 130\ V$



(e) $|V_{BCK}| = 140\ V$



(f) $|V_{BCK}| = 150\ V$

Figure 4.32: *Analog outputs of a MATISSE observed at the oscilloscope for different backside voltages. The voltage applied to backside is negative. The white line indicates the beginning of the readout phase. The four outputs have been shifted to avoid the overlaps. At the very beginning (a) all the read values are zero but then, when the backside voltage reaches 130 V, all the read values increase and reach the expected baseline of 400 mV. Outputs (b) and (c) show that the depletion starts from the inner region of the matrix.*

suggest that pixels receive at their input a constant and high current which generates a negative saturation. However, when the backside voltage further increases, the output voltage of some pixels starts to increase as well. The expected voltage in case of full depletion is the baseline of the channels which has been set to 400 mV. When V_{BCK} is equal to 110 V, the baseline of several pixels increases and goes around the expected value. However, in each sector the read values are divided into six groups by some very low outputs. The groups are the columns of the sectors and the low outputs belong to the pixels close to the matrix border. Even though the observed baseline of the inner pixels is around the expected value, in some cases, it is 50 mV higher or lower. Since at 100 V there is this wide baseline variability, the leakage at the input of the inner pixels is not negligible and thus the sensor can not be considered fully depleted. The effect of the borders is more visible in sector 0 and 3 (see Figure 4.32b) because the first columns in case of sector 0 and the last in case of sector 3, have a very low baseline. At this voltage, the area which receives a very high leakage involves three columns of both sectors, therefore, it extends at least for 150 μm from the matrix edges. When V_{BCK} reaches 120 V, the baseline variation is significantly reduced and the extension of the undepleted region decreases to 50 μm. This proves that when the depletion region reaches the silicon surface, it involves first the inner pixels and then it extends also to the borders. For this reason, the leakage observed is always bigger for pixels placed close to the periphery. However, when the backside voltage is equal or higher than 140 V, the leakage is reduced also at the periphery and all the pixels behave in the same way. This value is considered the depletion voltage of the detector because the undesired effects generated by parasitics inputs have been completely removed. This number is also in agreement with the C-V characteristic previously obtained and with what observed in the test structures built on the same wafer.

Bulk leakage current and punch-through voltage

The bulk leakage current has been measured from the back at different backside voltages by using the same setup scheme shown already in Figure 4.29. The I-V characteristic, shown in Figure 4.33, has been obtained in the dark and at room temperature. It is possible to divide the curve in three different regions based on the value of V_{bck}. The first one extends up to 180 V and here the measured current is low and ranges from about 0.5 nA up to 4 nA. In the second region, the current increases

rapidly up to 1 mA when 250 V are applied. However, the current trend in this region follows the one expected by an ohmic device of 1 MΩ which is compatible with the resistive path through the external region. For this reason, it is assumed that this additional current flows laterally to the depleted volume and is collected by the guard-rings. This is proved also by the pixel cells which do not saturate due to this current.

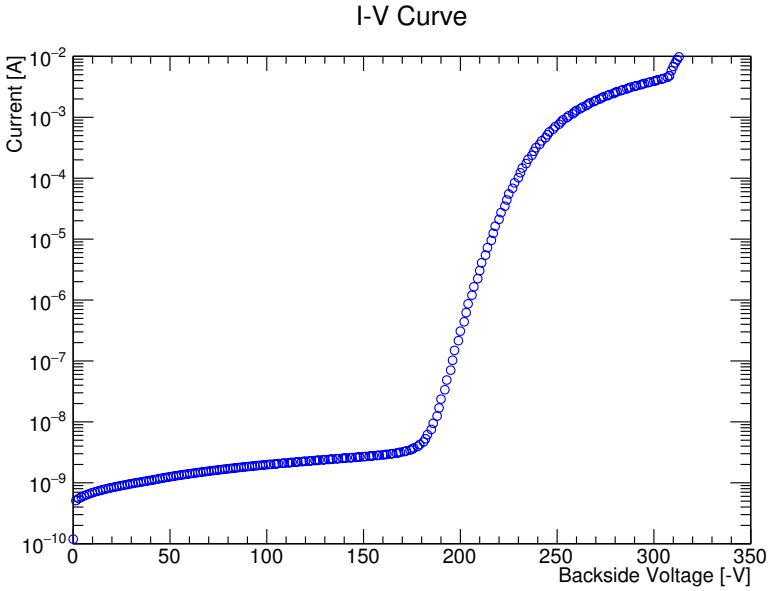


Figure 4.33: *Leakage current flowing through the p^+/n-substrate diode at different backside voltages*

The last region starts when V_{bck} is around 320 V. Here the current increases additionally following the trend of the 1KΩ resistor used to limit the current in the HV domain so this is assumed as the punch-through voltage. In this region all the cells go in saturation.

Figure 4.34 shows a comparison of leakage in samples from wafer 18 (called M18) and 19 (called M19) with backside voltages up to 200 V. The measurement has been carried out both in the dark and under illumination. Contrary to what observed in the dark with M19 where the leakage is below 4 nA up to 180 V, in M18 the leakage reaches few μA after only 40 V. Under illumination both samples behave similarly: an increase of the leakage over 10 μA is observed due to the charge generated on the surface by light photons. As expected, this measurement confirms once more the better performances of devices coming from wafer 19. As discussed

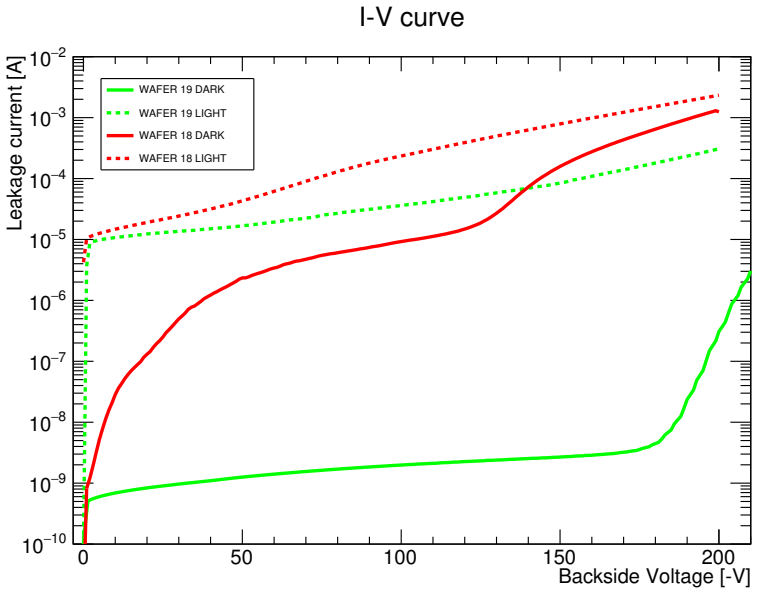


Figure 4.34: *Comparison of I-V curves obtained from wafer 18 and 19 in the dark and under illumination*

in the previous sections, these different performances are due to the different trapped-charge concentration in the backside ONO insulator which is higher in samples built on wafer 18.

To summarize, results from I-V and C-V characteristics from samples built on wafer 19 give a depletion voltage of -140 V. In this condition all the silicon surface where the matrix is built is depleted and thus, there are not free charges. As a consequence the leakage current is very low and around units of nA up to -180 V. For higher voltages, the measured current from the backside increases and flows through the chip edge without reaching the inputs channels because they are collected by the guard-ring on the top. The effective doping concentration of the substrate is 1×10^{12} cm^{-3} and has been measured by means of the $1/C^2$ trend. The punch-through voltage is measured around 280 V but most probably this values increases if the trapped charge oxide in the ONO is completely, or partially, removed by means of the irradiation of the test diodes.

4.3.2 Characterization of the readout electronics

Power consumption measurement

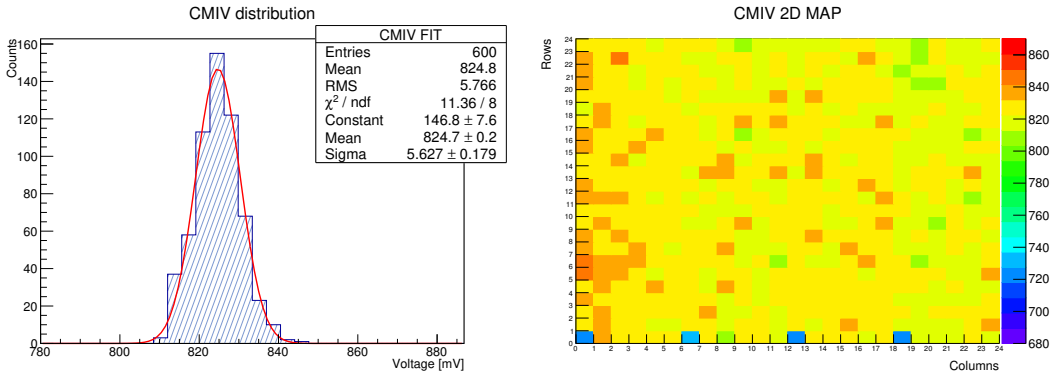
MATISSE has been designed in order to be very low power during all the operations of data taking and during the data transmission. The expected power consumption of the single channel is $\sim$6 μW during the static operations like the integration and sampling phases. In this condition, the expected power consumption for the whole matrix, taking into account also the contribution of the bias cells and the End of Column (EoC), is 4.14 mW. During the data transmission, two buffers per sector send data off-chip increasing the expected power to 13.8 mW.

In Table 4.3 the values of power consumption measured in the motherboard and in MATISSE are reported. The contribution from the main board can be measured since the power domains are separated in 1.2 V and $\pm$5 V. The $\pm$5 V domain is used to supply all the devices mounted on the board like transceivers, LDOs and voltage shifters. The power consumption here is about 2 W. For what concerns the 1.2 V domain, it is used to set some biases need by the ASIC. The power consumption measured in this domain is 540 μW. The measured values in MATISSE in static and dynamic conditions are a little bit lower than what expected but they contain neither the contribution from the digital part of the pixels nor the one of the EoC. In the static condition, the measured power consumption for each channel is 6 μW as expected from simulations.

SYSTEM	SUPPLY [V]	EXPECTED [mW]	MEASURED [mW]
motherboard	$\pm$5	-	2000
motherboard	1.2	0.57	0.54
ASIC (static)	1.2	4.14	3.84
ASIC (transmission)	1.2	13.8	13.2
Channel (static)	1.2	6×10^{-3}	6×10^{-3}

Table 4.3: *Power consumption measured in the main board and MATISSE.*

Measurement of the common mode input voltage in the very front-end



(a) **(b)**

Figure 4.35: *Distribution of the common mode input voltage measured in MATISSE (a) and its representation in the pixel matrix (b). The distribution amplitude is caused by noise and mismatch in the input transistor. The map shows that there are no dependencies on the physical position in the matrix array.*

Depletion and punch-through are strongly correlated to the common mode input voltage (CMIV) of the first stage of the analog readout. In general the higher is the value of this parameter, the lower is the depletion voltage and the higher is the punch-through voltage. So in principle, one would like to set the highest possible value to increase the electrical field and collect the deposited charge in the sensor faster. However, as explained in Chapter 2, this voltage is limited from one side by the technology and from the other side by the threshold voltage of the PMOS input transistor used in the front-end. For this reason, a trade-off has been found during the design and the value of 820 mV has been chosen as the best compromise. Since this element is so important both for the sensor depletion and to set the working operation point of the font-end, a dedicated measurement to check this voltage has been done.

In the regular operation of the detector, the input voltage cannot directly measured off-chip. However, if the matrix is kept under reset the CMIV can be read at the CSA output. In such a way, it is possible to get the desired information by following the regular readout procedure. This measurement has been done in the dark, at room temperature and at -160 V. Figure 4.35a shows the distribution of the CMIV among all the pixels of MATISSE. As expected, the values are distributed by following the normal distribution because of the electronic noise. The measured value of CMIV

is (824.7 $\pm$ 5.6) mV. The FWHM (full width at half maximum) of the distribution depends on the electronic noise but also by the dimension of the input transistor because it imposes the mismatch between all the pixels in the matrix. Montecarlo simulations predicted a sigma distribution of 4 mV for the CMIV, so the results are definitely in good agreement with the simulations. An interesting observation is that there is no dependency on the pixel position in the matrix as can be observed in the map of Figure 4.35. This is possible only because the leakage current coming from the sensor has been reduced thanks to the full depletion.

Linearity and dynamic range of the full readout chain

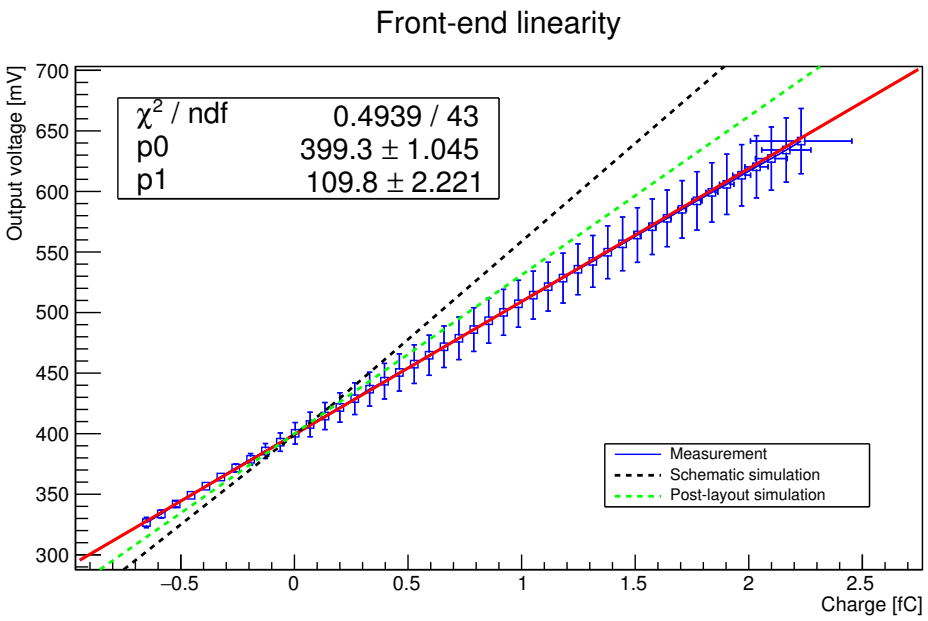


Figure 4.36: *Output voltage generated for different injected charges by means of the internal test pulse circuitry.*

The very front-end chain has been designed in order to readout charges up to 24 ke$^-$ with a very linear response. This has been done by maximizing the dynamic range and the linearity of each block of the readout chain. Thanks to the internal mechanism for injecting local test pulses, these quantities can be characterized without the use of real signals coming from the sensor. The amplitude of the pulses, and thus the injected charge, can be tuned by means of a trimmer placed on the motherboard. A measurement has been carried out generating local inputs in a sample kept in the dark and in full depletion at -160 V. Figure 4.36 shows the voltage

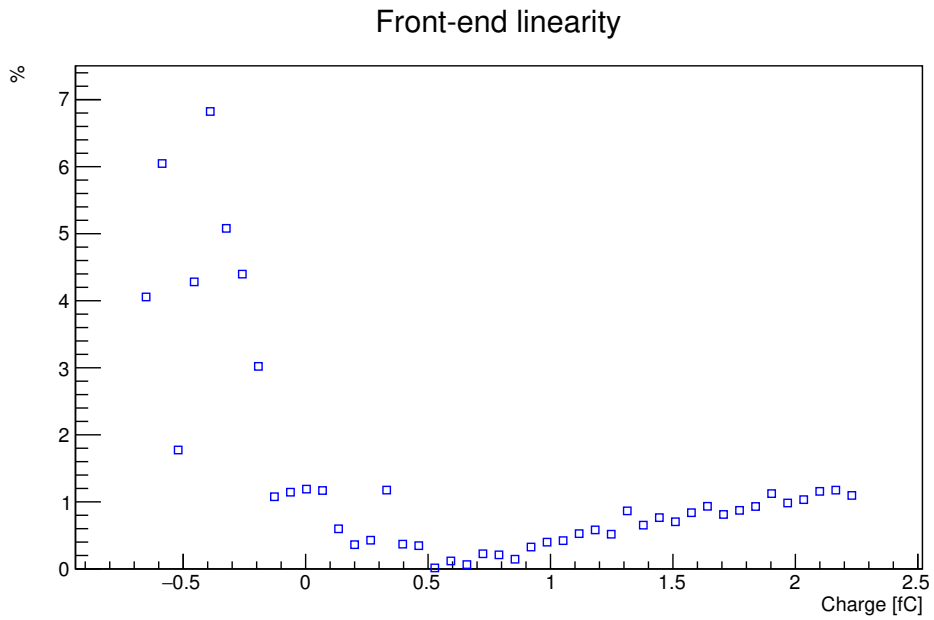


Figure 4.37: *Percentage of linearity of the analog readout implemented in the pixels of MATISSE. For negative charges the linearity reaches 7 % whereas for the positive ones is below 1 %.*

amplitude sent off-chip for input charges up to 2.4 fC, value which corresponds to the biggest pulse that can be generated. During the measurement, the baseline has been set to 400 mV. In this range of charge, the voltage output follows a linear trend with a difference from the ideal fit below 1 % for almost all the positive injected charge (Figure 4.37). Also negative charges have been injected to explore the region below the baseline. Here the percentage of linearity is worse (7%) but it is still acceptable in case a very wide dynamic range is needed. Those results are in good agreement with the simulations. It is also interesting to compare the measured output voltage with the trend expected by simulations. In schematic simulations indeed the expected analog gain is $\sim$150 mV/fC and in post-layout is $\sim$131 mV/fC. However, the gain obtained during the detector calibration (see section 4.3.3) is $\sim$116 mV/fC which is lower. The differences between these results are due to parasitics in the small feedback capacitance used in the pre-amplifier which reduces the analog gain. This reduction is visible also in post-layout simulations but the effect is bigger in the measurement.

Even though the gain is lower than expected, the results guarantee that the readout chain can work with a very linear response from about 400 mV up to

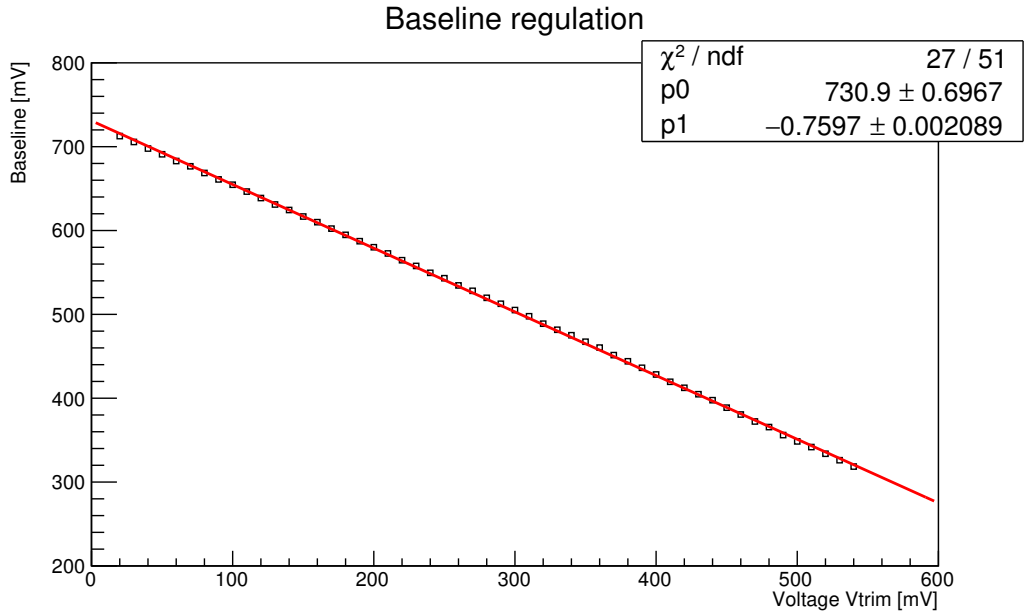


Figure 4.38: *Baseline tuning by means of the trimmer on the main board*

700 mV, revealing a wide dynamic range for a 1.2 V CMOS technology. From simulations is expected a good linearity up to 800 mV but unfortunately, the test pulse mechanism does not allow to explore this region of voltages due to the lower gain.

An additional feature of MATISSE that can be used to study dynamic range and linearity of the channel is the tunable baseline described in the previous chapter. Based on a voltage set on the motherboard by means of a trimmer V_{TRIM}, it is possible to regulate the baseline as desired in a range between 400 mV and 800 mV. The plot of Figure 4.38 shows how the regulation behaves. The maximum baseline of 710 mV is obtained with the minimum trimmer voltage. It reasonable to think that, also the small capacitance used to tune the baseline has been affected by parasitics, as has been observed in the feedback capacitance. This explains why the minimum regulation is lower than the CMIV (820 mV). Also this effect was predicted by simulations. When V_{TRIM} increases, the charges are injected at the channel input and the baseline moves down. In the measurement, the baseline has been regulated up to $\sim$320 mV revealing an excellent linearity and a wide dynamic range of $\sim$400 mV. Thanks to these properties the in-pixel electronics could be used to readout both sensor polarities to detect input charges up to $\sim$21.5 ke^- which correspond to the X-ray energy of 70 keV.

Electronic noise measurements

The noise of the very front-end is a fundamental parameter which must be measured with high precision. For this reason, a dedicated study has been carried out to estimate first the electronic noise contribution coming from the different parts of the data acquisition system used for the characterization. The measurement has been done by means of the four ADCs mounted in the DAQ-box and thus allows also to observe non-uniformities (pedestals) between the channels. Noise is measured sampling several times the output voltage generated by the configuration under test. In such a way the measured voltage is represented by a Gaussian distribution where the standard deviation is the electronic noise of the system under study [64]. The tested configurations are the different parts of the full chain of data acquisition: the DAQ box, the DAQ-box connected to the motherboard, the DAQ-box connected to the motherboard and mezzanine and to conclude the full chain with a detector mounted. The measurement was controlled by the software developed to control the DAQ box. Table 4.4 reports the measured noise at the different levels of the chain.

DEVICE	NOISE [ADC]	NOISE [mV]	NOISE [e^-]
DAQ	0.2	0.014	0.75
DAQ, MB	0.2	0.014	0.75
DAQ, MB and mezz.	1.6	0.112	6.0
DAQ, MB, mezz. and ASIC	14.3	1	54

Table 4.4: *Noise contribution from different parts of the data acquisition chain. The contribution of the boards has been evaluated with all the discrete electronics in operation. (1 ADC count = 0.07 mV). Electrons are evaluated by means of the analog gain $A_{Q\rightarrow V}$ = 116 mV/fC*

It clearly appears that the noise contribution from the DAQ box and motherboard can be considered negligible because in the order of few μV. More important, but still very low, is the contribution coming from the mezzanine which is $\sim$110 μV (6 e^-). These values prove that the resolution of the DAQ system is high enough for the ASIC characterization with high precision. In the complete configuration, a detector has been tested in the dark and in the condition of full depletion at -160 V. The digital control signals have been set in order to read the baseline of the channels. The measured electronic noise is around 14.2 ADC counts which correspond to

$\sim$1 mV (54 e^-). This value is compatible with the expected one from simulations (900 μV). The electronic noise distribution between all the pixels of the matrix (reported in Figure 4.39) shows that the channels have similar performances in terms of noise. Indeed 96 % of the total number has a noise between 11 (38 e^-) and 17 ADC counts (65 e^-). Figure 4.40 shows the noise distribution of each sector. Even though the pedestal subtraction has been done before the measurement to remove initial offsets among the four sectors, they still present a small difference in terms of noise. In the tested sample, sectors 0, 2 and 3 have similar noise distributions with a very low noise around 36 e^-. What measured in sector 1 is a little bit higher (42 e^-) most probably because of the nwell shape used in this sector which increases the sensor capacitance.

Electronic noise has been measured in different samples built in the same wafer obtaining similar results and reported in 4.41. Only in samples where uniformities in the depletion are visible, most probably due to the trapped charge on the oxide, the bar error of the measured noise is much higher. This is the case of sample 2 in the figure where it has been observed a high leakage current. For the same reason, very high noise has been measured also in samples built on wafers 18 and 24.

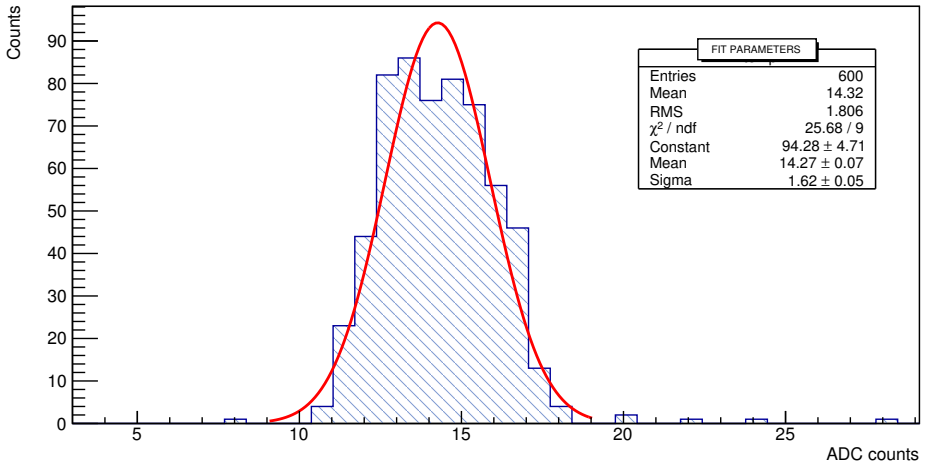


Figure 4.39: *Noise distribution of the pixel matrix of a sample built on wafer 19. The X axis is in ADC counts. (1 ADC count = 0.07 mV)*

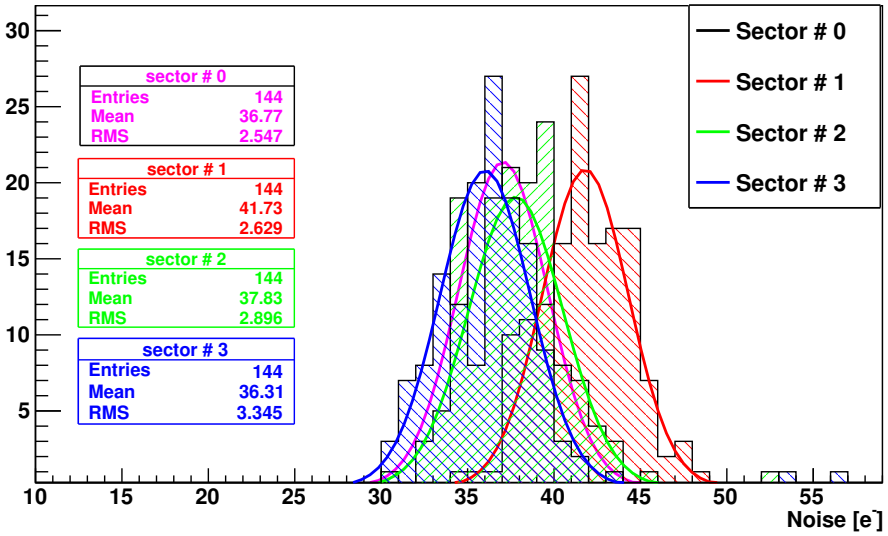


Figure 4.40: *Noise distribution in the sectors the MATISSE. Sectors 0, 2 and 3 have similar results with a noise mean noise around 36 e^-. In sector 1 the mean noise is 42 e^-*

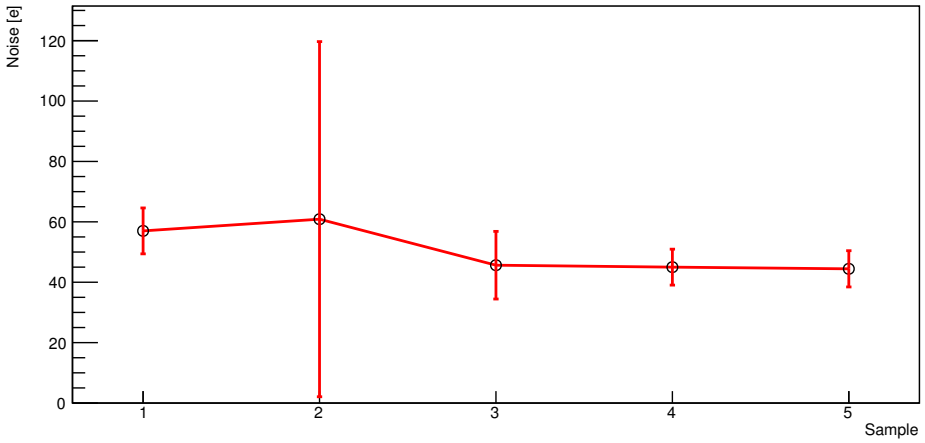


Figure 4.41: *Noise of the whole matrix measured in different samples from wafer 19. Noise is estimated from the fluctuation of the baseline*

Noise has also been evaluated at the pixel level by means of the internal test pulse by sampling the output of a random pixel with an oscilloscope. The positive slew rate SR^+ and the jitter σ_t of the signal generated by the pulse have been measured and then the electron noise σ_V has been calculated off-line following the formula 4.4.

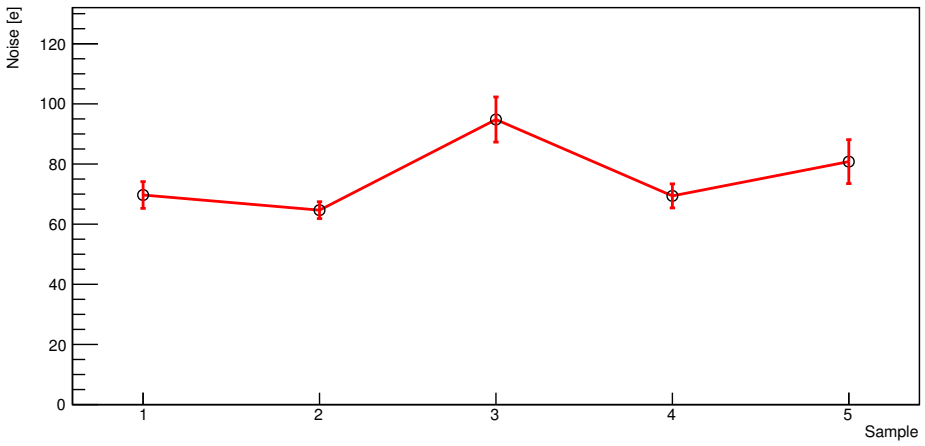


Figure 4.42: *Noise in single pixels randomly chosen by means of internal pulses*

$$\sigma_V = SR^+ \times \sigma_t \tag{4.4}$$

The tested pixel has been chosen randomly and the measurement has been repeated with five samples at room temperature and at -160 V. Figure 4.42 shows that all of them have a similar noise. In this case also the error bar of the electronic noise measured in sample 2 is similar to the others because the chosen pixel belong to a region of the matrix array where there are no uniformities. The measured values are around 70 e^- which is still compatible with the expectations. The error bars in the plot have been obtained from the sensitivity of the oscilloscope.

Effects of digital noise injection

The circuitry built in the pixel contains a dedicated structure used to validate the integration of both analog and digital electronics in a small area of 50 μm $\times$ 50 μm. This structure is a simple chain of digital buffers which can be used to emulate the presence of a very fast digital electronics in the pixel. A dedicated measurement has been done in this large buffer, injecting at its input a digital square with different frequencies. Noise at end of the analog readout chain is measured to identify any kind of induced noise by the digital block. Figure 4.43 shows the results obtained with frequencies up to 1.6 MHz. The contribution coming from the digital circuitry can be considered negligible. This result proves that the technology allows the integration

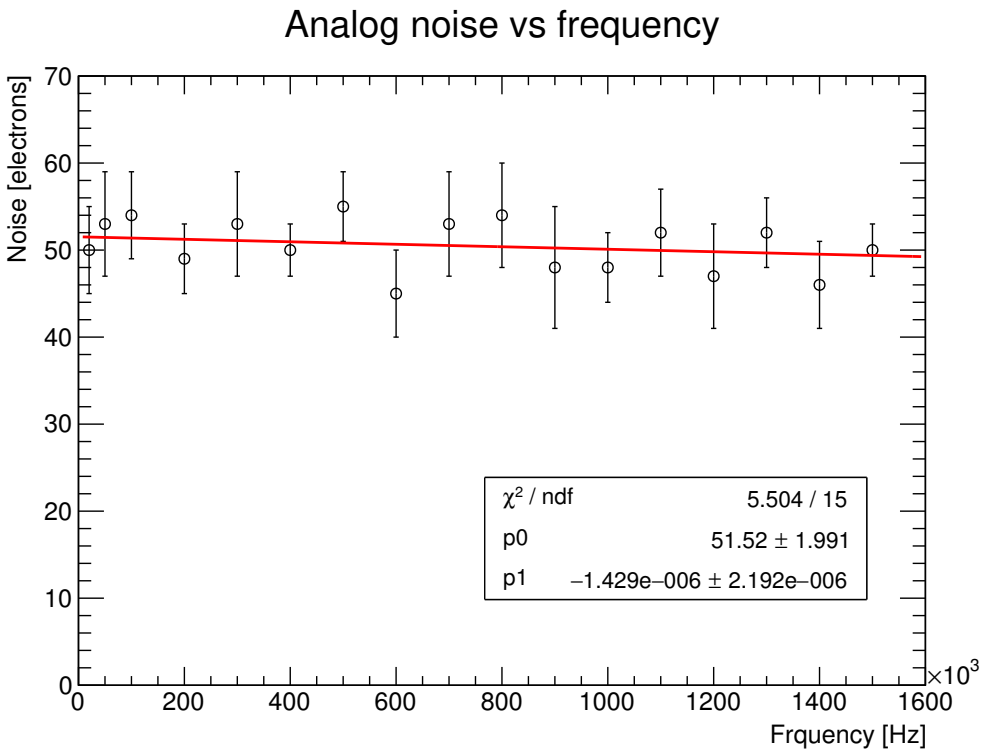


Figure 4.43: *Measurement of noise with a fast digital electronics working in the pixel at different frequencies*

of a fast digital electronics with the analog circuitry without any degradation of the performances.

Measurements of information loss

The information about the released charge in the sensor is stored as a voltage in two capacitors placed in each pixel unit. This voltage slowly decreases due to the effects of leakage currents flowing through parasitics which unavoidable forms undesired discharge paths. In general the two stored voltages decrease slowly with the same RC constants because the CMOS electronics layout around those nodes is identical. Therefore, the difference between the two values should be constant. However, the leakage current of MIM capacitors depends also on the voltage drop around the capacitor itself and so high stored voltages will decrease faster than low voltages. Since in p-type sensors, the baseline is lower than the signal, their difference will not be constant in time, thus generating information loss. An easy way to limit this

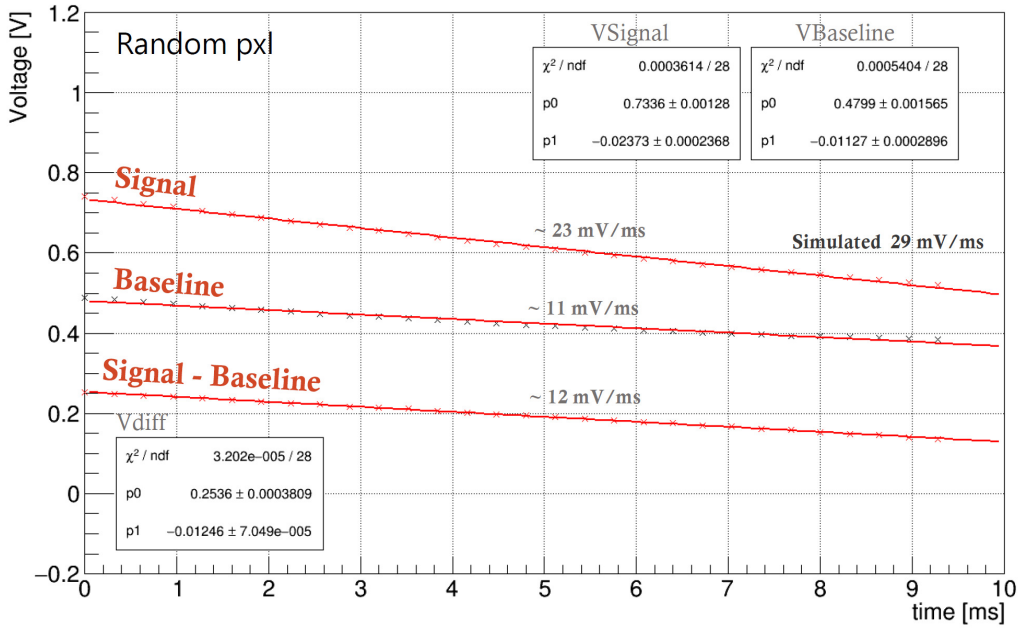


Figure 4.44: *Transient measurement of the stored voltages in a random pixel of the matrix*

effect is reducing the dead time of the sensor with the use of a fast clock for the readout. MATISSE has been designed to work with a readout clock of 5 MHz which allow to readout the full matrix in 28.8 μs.

A dedicated measurement has been done to estimate the information loss in a pixel randomly chosen from the matrix. The sampled voltages are the baseline of the pixel and the output generated by a local pulse. The two stored voltages are acquired by means of an oscilloscope to observe their transient variations. Picture 4.44 shows the behavior of the stored voltages in 10 ms. As expected the signal generated by the test pulse drops much faster than the baseline and thus also the difference V_{pulse} - $V_{baseline}$ changes. At the nominal clock, the expected voltage drop for the last pixels of each sector is 350 μV which corresponds to $\sim$19 e^- which is negligible if compared with the measured noise.

For applications where a lower speed is used, for instance 1.25 MHz, the expected information loss is $\sim$75 e^- which is higher than noise. In this case in the analog signal generated during the data taking will present a not negligible voltage drop which increases as long as the pixel is closer to the last pixel of the last column. In Figure 4.45a is reported, as a real example, the analog outputs obtained during a measurement of the common mode input voltage with a clock frequency of 1.25 MHz.

In the four sectors, the voltages read from the last pixels have a lower value because of the information loss during the readout procedure. This effect can be mitigated by an off-line correction as shown in Figure 4.45b.

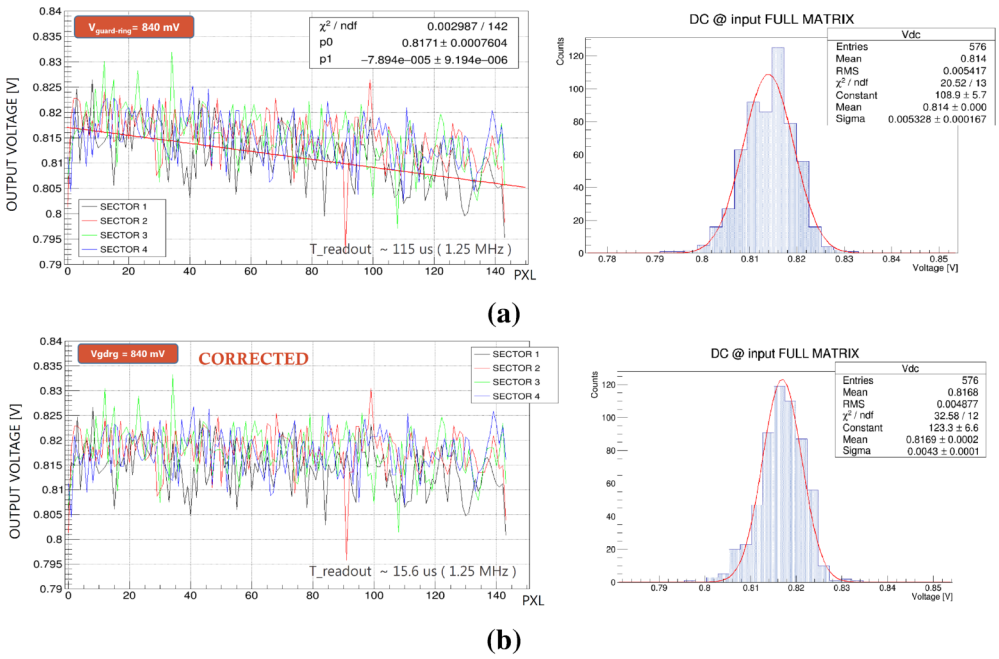


Figure 4.45: *Common mode input voltage measured in the sectors of MATISSE with a clock of 1.25 MHz. For each sector is indicated the measured value of all the 144 pixels. At the top the original measured values (a) where a not negligible voltage drop is visible for the last pixels. At the bottom, the corrected values (b).*

4.3.3 Characterization of the system sensor-electronics

Calibration with X-rays sources

Each detector must be calibrated before being used to measure radiation. The calibration of the device allows to establish the relation between the output amplitude and the deposited charge in the sensor. Ideally, the test pulse injection circuit implemented in MATISSE could be adapted for the calibration of the readout electronics. However, the test capacitor used to inject charge at the input of the channels depends on the process used to built the electronics and therefore it is not known accurately enough for the calibration. A good tool which can be used for the calibration are X-rays sources because they produce very narrow energy bands which allow to study the detector performance at different and well-known energies. When an X-ray photon reaches the depletion region of the sensor it primarily interacts with the semiconductor through photoelectric effect. Since it has an energy bigger than the band gap of silicon (3.6 eV), the result of this interactions is the generation of electron-hole pairs. In general, the higher is the incoming energy, the higher is the number of pairs produced [65]. MATISSE has been calibrated by means of two different X-rays sources: ^{55}Fe and a X-ray tube. The results obtained with these sources are reported in the following sections.

Measurements with the radioactive isotope ^{55}Fe The monolithic sensor has been tested with a laboratory source of X-rays in order to evaluate the sensor performance and to calibrate its gain. The source used for the measurements is the ^{55}Fe, which has the spectrum with two characteristic peaks as reported in Figure 4.46. This radioactive isotope decay by electron capture to ^{55}Mn. The most important decay transitions generate the emission of Auger electrons, K-alpha and K-beta X-rays lines. Auger electrons are emitted with an energy of 5.19 keV and a probability of 60 %. The K-alpha lines are two, K-alpha-1 and K-alpha-2, and are emitted with an energy of $\sim$5.899 keV and $\sim$5.887 keV respectively. Since the K-alpha X-rays have similar energies, they are often considered as a single peak released with a probability of 24.4 %. The remaining component is the K-beta line which is released with a nominal energy of 6.49 keV and a probability of 2.85%. Usually, Auger electrons are blocked by means of a thin kapton films which are transparent to the X-rays and thus they are not visible in the final spectrum [66].

When the ^{55}Fe X-rays photons reach the detector, it deposits all its energy in a silicon layer few micrometers thick generating 1625 and 1787 electron-hole pairs with X-rays of 5.89 keV and 6.49 keV respectively.

During the data acquisition, events are collected in clusters in order to store only useful data. The single cluster is composed of 5×5 pixels built around a seed pixel where a threshold of $5 \times \sigma_V$ is applied. In the other pixels of the cluster a threshold of $2 \times \sigma_V$ has been used . Electronic noise is about 38 e^- in the sample used for the measurement. Figure 4.47 shows the spectrum reconstruction of a depleted sample by means of the four sectors used independently. The measured peaks are around 440 and 450 ADC counts for all the sectors. The secondary peak should be around 494 ADC counts but it is covered by the background.

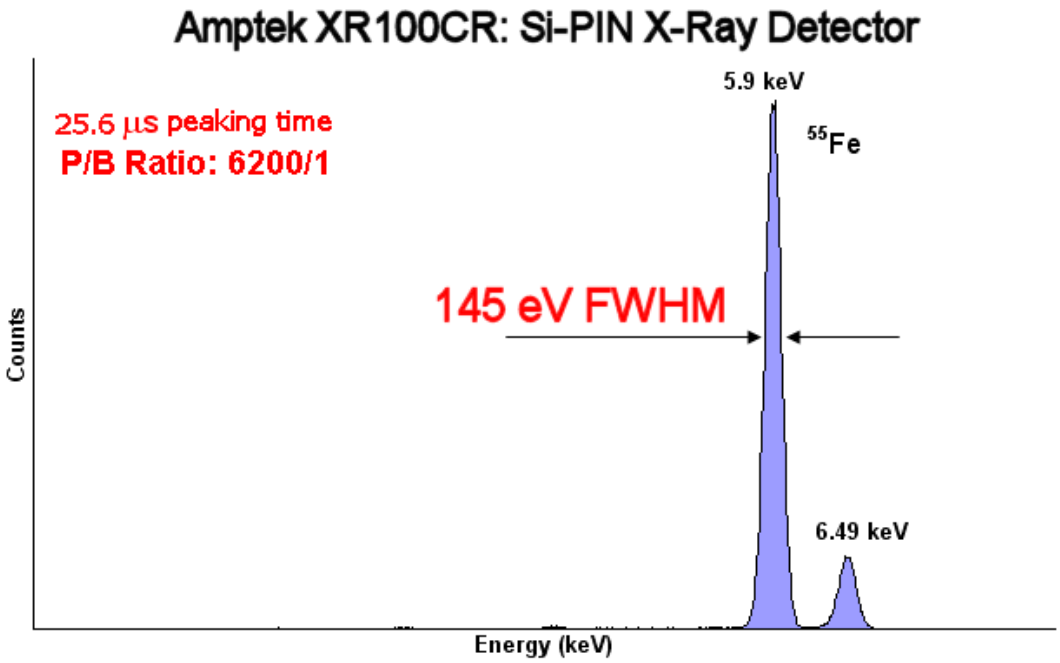


Figure 4.46: *Fe^{55} spectrum taken with a 6 mm^2/500 µm Amptek XR100CR Si-PIN detector [67]*

Table 4.5 resumes the measured peaks and the calculation of the analog gain expressed in mV/e^- and in mV/fC.

By using those values the calculated mean analog gain is:

$$A_{Q\to V} = (120.6 \pm 5.8)\ mV/fC = (19.29 \pm 1)\ mV/ke^- \tag{4.5}$$

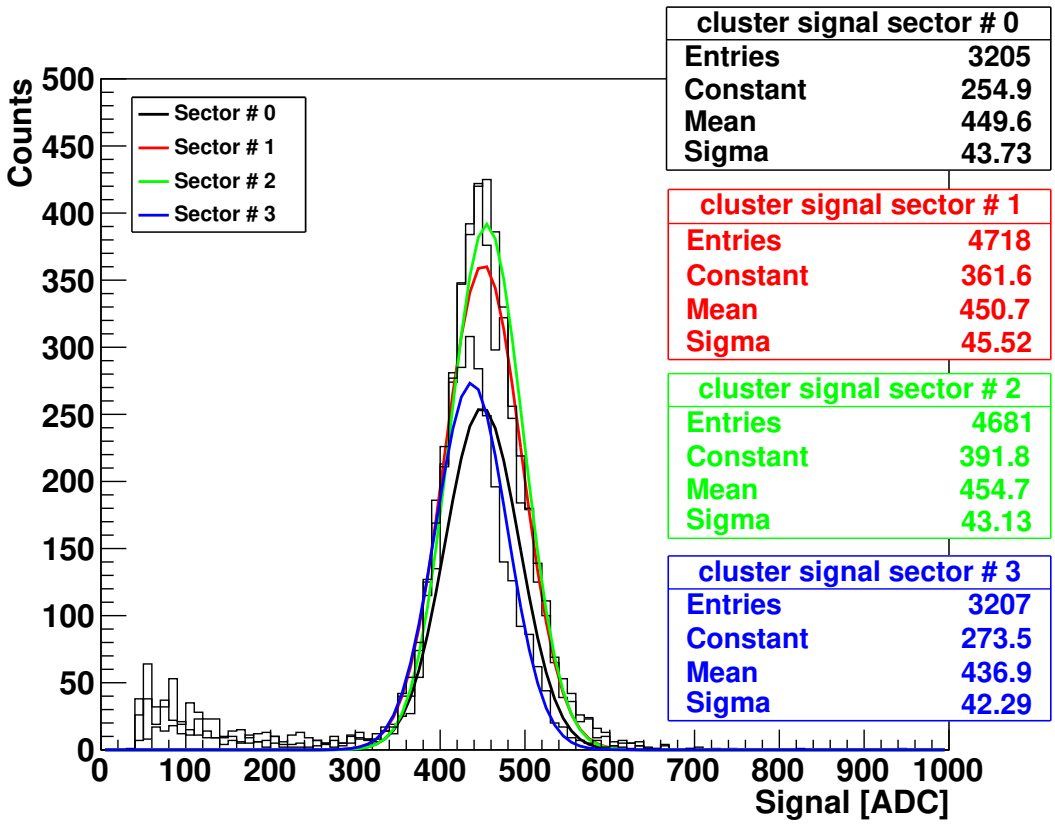


Figure 4.47: *Data acquisition with a ^{55}Fe sources on the four sectors of MATISSE.*

				Measured peak					
Source	**Energy [keV]**	**Q_c [e$^-$]**	**Q_c [fC]**	**Mean [ADC]**	**Sigma [ADC]**	**Mean [mV]**	**Sigma [mV]**	**$A_{Q\to V}$ [mV/ke$^-$]**	**$A_{Q\to V}$ [mV/fC]**
^{55}Fe$_{S0}$	5.9	1638	0.26	449.6	43.7	31.5	3.1	19.2	121.2
^{55}Fe$_{S1}$	5.9	1638	0.26	450.7	45.5	31.55	3.19	19.3	121.4
^{55}Fe$_{S2}$	5.9	1638	0.26	454.7	43	31.83	3.01	19.4	122.5
^{55}Fe$_{S3}$	5.9	1638	0.26	436.9	42	30.58	2.94	18.7	116.7

Table 4.5: *Peaks observed with the active source ^{55}Fe. Q_C in the table is the expected collected charge in silicon when the radiation crosses the sensor. The measured peak in each sector is reported in ADC counts and in mV (1 ADC count = 0.07 mV).*

Measurements with a X-rays tube The spectrum of an X-ray tube is composed by the characteristic emission lines of tungsten and by the bremsstrahlung spectrum which starts at low energies and reaches a maximum determined by the potential

applied to the tube. This spectrum can be modified by means of filters which allow isolating narrow energy bands of X-rays [68]. MATISSE has been calibrated by means of the facility for total dose RP-149 Semiconductor Irradiation System at INFN Padova [62]. The machine has been specifically modified to reduce the dose rate and to get a monochromatic spectrum by means of a monochromator. Two different energies have been selected: 7 KeV and 8.7 KeV.

MATISSE has been tested under X-rays by selecting an integration time of $\sim$13 μs with a readout clock of 3.12 MHz. The sensor has been fully depleted with a backside voltage of -160 V. To set the thresholds needed by the cluster acquisition, the electronic noise has been estimated before the measurement around 12 ADC counts (0.84 mV). Figure 4.48 shows the noise distribution in the matrix array used for the measurement.

For each energy, the spectrum has been first reconstructed by means of a reference detector: the Amptek XR-100CR. In Figure 4.49b the spectra obtained with the two energies are reported. The first one has a peak at 7 KeV and a tail towards high energies. The second one is more symmetric and has a clear peak around 8.7 KeV. The ratio between the two measured peaks is $\sim$0.71. The figure clearly shows how the monochromator cuts the bremsstrahlung spectrum generated by the tube and selects a narrow band of energies.

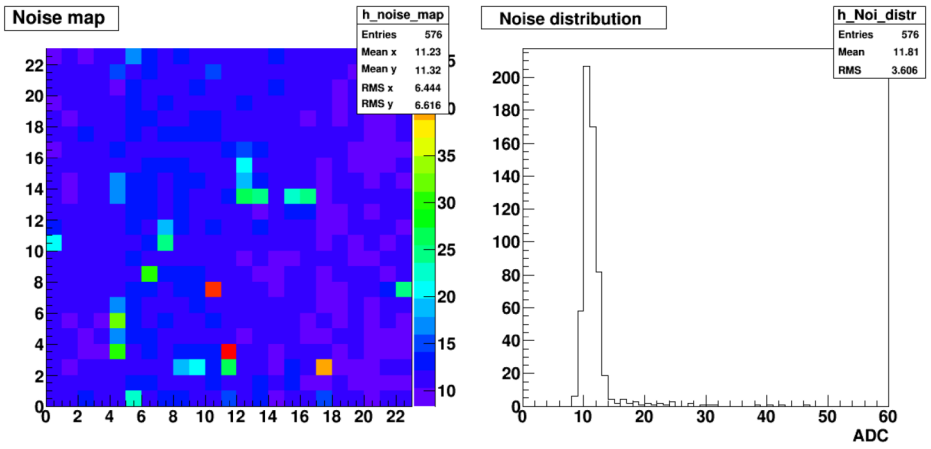
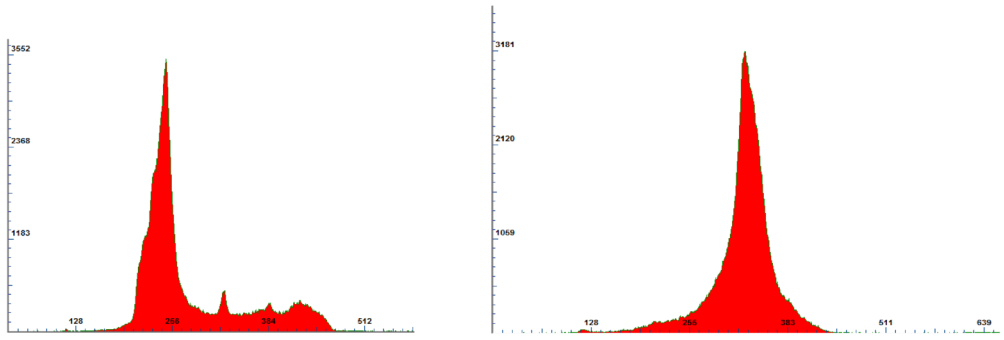


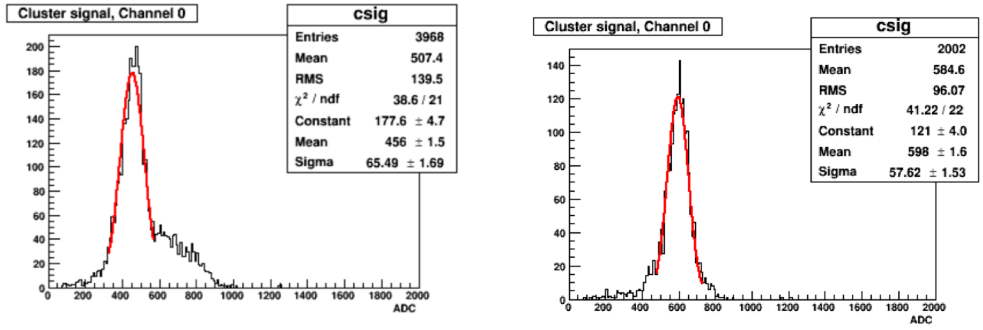
Figure 4.48: *Map reconstruction during the noise measurement on the left (a) and noise distribution among 576 pixels on the right (b)*

The X-ray spectrum has been then reconstructed by using the four sectors of MATISSE. In order to filter noise during the data acquisition, a threshold equal to



(a) **(b)**

Figure 4.49: *Spectrum obtained through the XR-100CR with the selected energies of 7 keV (a) and 8.7 keV (b)*



(a) **(b)**

Figure 4.50: *Spectrum obtained with MATISSE. On the left the one obtained with an energy of 7 keV (a) and on the right with 8.7 keV (b)*

$7\times\sigma_V$ has been set on the seed cluster. In Figure 4.50 the reconstructions obtained with tens of thousands of events detected by the first sector of MATISSE are reported. The spectrum obtained with 7 keV reflects the one obtained with the Amptek XR-100CR. It is asymmetric with a tail towards high energies and has a clear peak around 456 ADC counts. The second spectrum is also in good agreement with what obtained with the commercial detector. In this case, the peak is around 598 ADC counts. The ratio between the measured peaks is 0.76 which is comparable with the 0.71 obtained with the Amptek XR-100CR.

In Table 4.6 the important numbers obtained by the spectra together with the analog gain calculated for each energy based on the expected collected charge Q_c are resumed.

			Measured peak				Gain	
Energy [keV]	**Q_c [e^-]**	**Q_c [fC]**	**Mean [ADC]**	**Sigma [ADC]**	**Mean [mV]**	**Sigma [mV]**	**$A_{Q\to V}$ [mV/e^-]**	**$A_{Q\to V}$ [mV/fC]**
7	1939	0.31	456.0	65.5	31.92	4.59	16.4	103.0
8.7	2416	0.387	598.0	57.6	41.79	4.03	17.3	108.0

Table 4.6: *Peaks observed with the X-ray tube. Q_C in the table is the expected collected charge in silicon when the radiation crosses the sensor. The measured peak is reported in ADC counts and in mV (1 ADC count = 0.07 mV). For each energy the gain has been calculated and expressed both in mV/e^- and mV/fC.*

After the measurements with X-rays and by means of ^{55}Fe, the following values of gain has been found:

$$A_{Q\to V,(^{55}Fe),5.8\ keV} = (120.6 \pm 5.8)\ mV/fC \tag{4.6}$$

$$A_{Q\to V,(X-R_{tube},7\ keV)} = (103.0 \pm 14.8)\ mV/fC \tag{4.7}$$

$$A_{Q\to V,(X-R_{tube},8.7\ keV)} = (108.0 \pm 10.4)\ mV/fC \tag{4.8}$$

Taking into account all these values, a good estimation of the gain is obtained by the weighted mean as follows:

$$A_{Q\to V} = \frac{\sum \frac{A_{Q\to V,i}}{\frac{1}{\sigma_A^2}}}{\sum \frac{1}{\sigma_A^2}} = (116.0 \pm 4.8)\ mV/fC = (18.6 \pm 0.7)\ mV/ke^- \tag{4.9}$$

This final number is what has been used everywhere in this thesis where it was required to express the information in electrons.

Laser measurements

The topside of MATISSE has been designed to allow the illumination of the sensor from the top by means of a laser source. The routing of the pixel unit in particular, has been done reducing to the minimum allowed by the DRC rules the metallization which may filter the light coming from the top. Figure 4.51 shows the final arrangement of the fillers in the pixel unit.

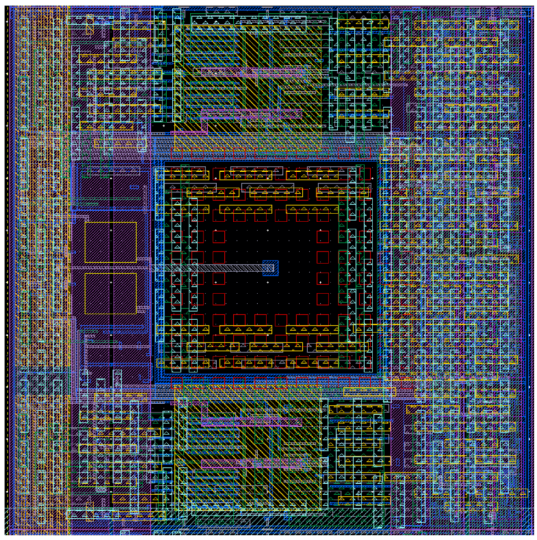


Figure 4.51: *Layout of the pixel cell. The rectangular shapes with triangles inside are the metal fillers which have been placed manually minimizing the metal density in the inner region.*

An infrared diode laser developed at CERN with a wavelength of 1060 nm has been used to study the performance of MATISSE. The optical fiber used for the signal transmission has been connected to a mechanical support capable to move in x,y and z with a precision of 10 μm. In such a way, by moving the fiber in the xy plane it is possible to test different regions of the matrix and by tuning the z coordinate it is possible to change the spot size. The integration time for the measurement has been set to 10 μs and a 3.25 Mhz clock has been used to readout the matrix array. The detector has been biased to -160 V and it has been kept in the dark on a anti-vibration table. The laser is controlled by the DAQ system which produces a trigger signal to drive the laser pulse generation. The trigger is generated after the sampling of the matrix baseline. The z coordinate has been set in order to have a very large spot which has been reconstructed in Figure 4.52. The reconstructions show that the pixel matrix detects quite well the signal with an optimal suppression of noise in those pixels where the signal is not present. In the measurement, the total charge collected is the integral of the signal amplitude on the x-y plane. By using the charge to voltage gain measured as explained in the previous paragraph, the total charge collected has been estimated equal to 31.25 fC ($\sim$195 ke^{-}). This charge is collected by 226 channels from the sectors in the middle of the matrix.

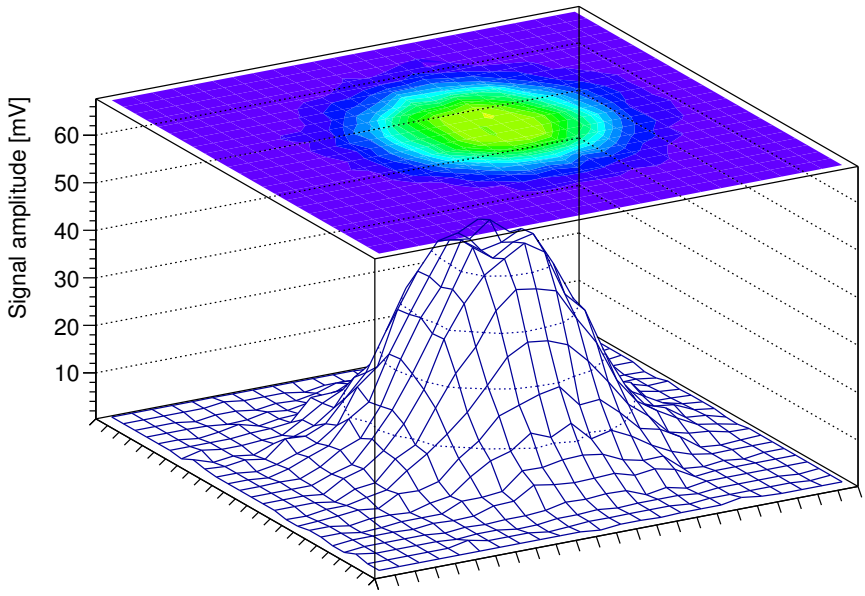


Figure 4.52: *Big laser pulse reconstructed with MATISSE*

A second measurement has been carried out with a smaller laser spot obtained by means of lenses designed to focus and to homogenize the laser beams below 10 μm of diameter. The intention was measuring the collected charge generated by the laser beam in different positions of the matrix array. Four positions of the second column of each sector have been studied. During each measurement, 160 hits have been sent in the middle of the selected pixel in order to evaluate the collected charge and its uncertainty. The middle point of the pixel has been found by means of a fine laser scan and it has been chosen as the position which minimizes the laser spot. To map the other 15 positions simple steps in x and y equal to the pixel pitch (50 μm) have been used. It has been observed that if the laser moves even by few μms the spot size increases significantly. So most probably even though the metal density on the top side has been minimized, the metallizations cause scattering which does not allow to focus the laser beam to the minimum. In Figure 4.53 the signal reconstructions obtained with the selected positions are reported. The plots are arranged based on the position in the matrix therefore, the four columns correspond to the reconstructions done in the four sectors.

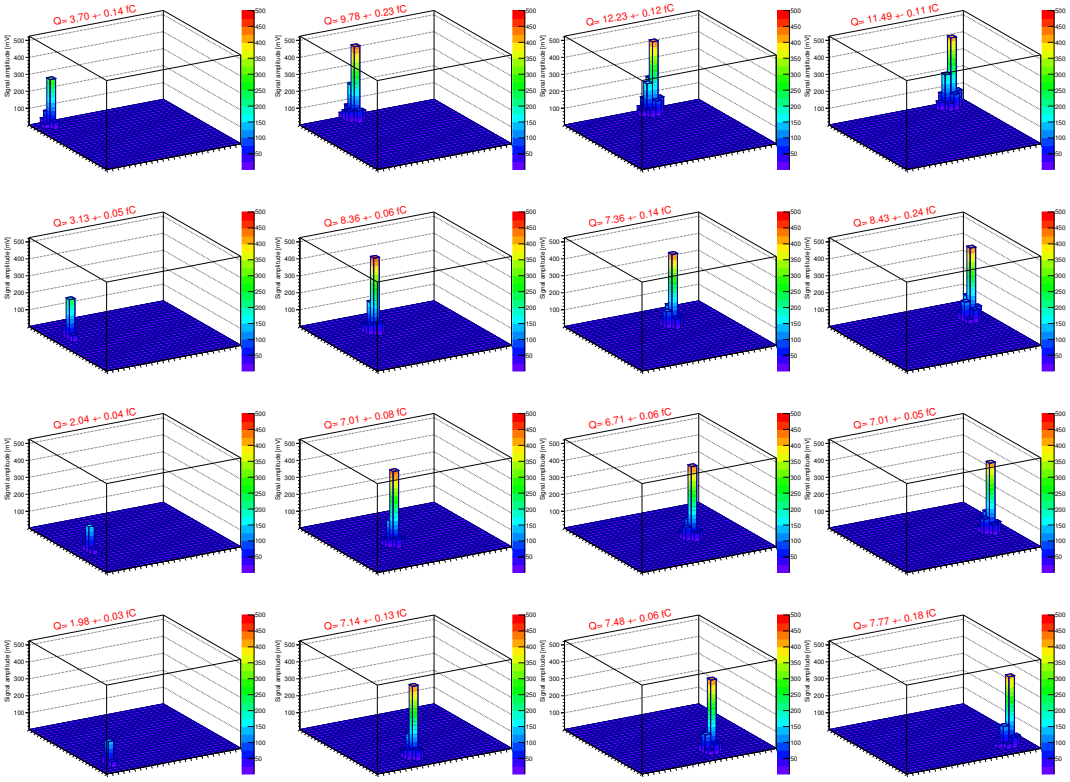


Figure 4.53: *Small laser spot reconstructed with MATISSE (a) and matrix array with a small laser pulse injected from the top (b)*

In all cases, the reconstructed spot is significantly much smaller than the big pulse of Figure 4.52 but in none, it was possible to reach the minimum size of 10 μm. Indeed, in most of the cases, the charge is collected at least by two or three pixels. For each position, the collection charge is measured with a high precision which in some cases reaches 0.03 fC (190 e^-) in 160 hits. An interesting thing to notice by looking the plots of the Figure 4.53 is that the collected charges in the four positions of sector 0 are similar and around 3 fC but they are much lower than the 8 fC collected in the other sectors. A more clear view of these results can be seen in the plot of Figure 4.54 where the charges collected in the 16 positions with their error bars are reported. The measurements, for the sake of clarity, have been divided based on the sectors and are shown with different colors. The order used to show the results respects the scan direction used during the measurement. The Figure 4.54 shows that unexpectedly, the values measured in sectors 1, 2 and 3 even though they are similar, are not distributed randomly around a mean value but it is visible a dependency from the position. Since it has been observed that scattering

on the top is present due to the metallizations, this leads to the hypothesis that there was a miss-alignment between the pixel matrix and the x-y plane used to move the spot that during the measurement. The difference of charge collected in the same sector in such a way is explained by the different position of the laser spot and thus by different deposited charge in the sensor. The same pattern can be observed also in sector 0.

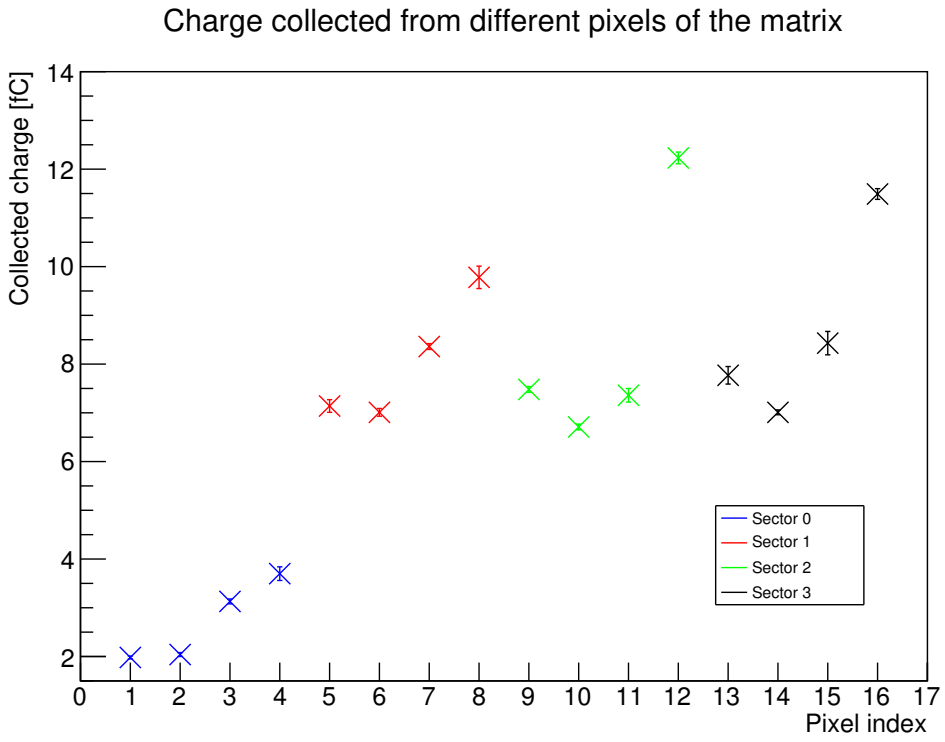


Figure 4.54: *Collected charge in 16 different points of the matrix array*

Chapter 5

Conclusions and future perspectives

In this thesis the development and the characterization of a novel low power CMOS monolithic active pixel sensor have been described. The device has been designed and fabricated in order to overcome the limitations of conventional monolithics sensors. During the design, the attention has been focused on the depletion volume trying to obtain a fully depleted device beyond 300 μm with a good reliability which is considered very difficult for the existing technologies. It has been discussed the limitations of the standard process in the development of this kind of sensors to motivate the needed of a custom fabrication. This has been made possible thanks to the close collaboration with an Italian Foundry which shared its experience of several years in the field of CMOS image sensors. The fabrication has been done with the double-sided processing in a 110 nm CMOS BSI technology. The backside has been fabricated with a modified processing whereas the front side with a standard CMOS processing. Two prototypes have been developed in order the characterize the technology and to prove the full depletion of the device. The characterization of the test structures focused on the sensor depletion and to estimate the leakage current. In test diodes and matrices the measured full depletion is around -140 V and the leakage current at this voltage is roughly 40 nA/cm^3. Radiation testing campaign results are very promising and show a good radiation tolerance of diodes up to 10 Mrad. The quality inspection of the backside layer performed with the MOS capacitor built on the backside, shows different properties of the oxides used to produce the three wafers. As a consequence of this, it has been observed the existence of trapped charge in oxide which limits the operation of the guard-rings built around the diode. The irradiation tests on the MOS capacitor, proved this theory.

The solution to overcome this effect has been found and consists of using a thicker oxide layer. The readout electronics of MATISSE, the second demonstrator, has been designed in order to integrate a versatile tool to prove the full depletion and the good integration of a CMOS electronics in the small pixel of 50 μm $\times$ 50 μm. Moreover, it has been designed in order to qualify the isolation between the electronics and the substrate. The characterization of the readout electronics show a good agreement with the simulations and this proves the good isolation realized by means of the deep-pwell implantation. All the features implemented in this prototype have been tested and the expected behavior has been observed. The readout chain allows the detection of charges up to 2.4 fC with an excellent linearity. Noise measured at the end of the chain is 40 e^-. Moreover, the digital test structure placed in each channel proves that the in-pixel electronics allow the implementation of both analog and digital domains without any kind of injected noise. The properties of the monolithic sensor have also been tested with X-rays sources and a laser source. The irradiation with monochromatic energies has been used for the calibration of the device. The reconstruction of the ^{55}Fe spectrum obtained with MATISSE shows a good agreement with the one obtained with a reference detector. Measurements performed with a focused laser beam show that charge induced in the sensor is collected by small clusters as expected by sensors where the charge is collected by drift. All these results are considered very prominent and a very important step in the development of monolithic sensors suitable for HEP experiments.

In the next future it is planned to conclude the characterization of the prototypes measuring some quantities like the collection time and the leakage injected in the pixels. In order to study more in detail the charge collection and quantify the depletion between two neighbor pixels, dedicated laser measurements are also planned. Studies of radiation damage with neutron (IEL and NIEL) are planned to quantify the radiation tolerance of the device. To conclude the characterization, also a beam test is planned to study the performance of MATISSE with ionizing particles. The good results obtained with these first prototypes allow to move towards a new generation of monolithics sensors where the limitations of the conventional MAPS have been overcome. More sophisticated devices with the same properties of full depletion but with a more complex digital circuitry on board will be developed. In this context, the project aims to explore also more sensor thicknesses in order to develop devices suitable to cover the wide range of applications which can take benefit from this low-cost technology.

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